MM56 Series CMOS (CD4000)

Equivalent to the RCA/Motorola Range
Dissipation typically 10 nanowatts per Gate
Temperature Range —40°C to +85°C

GENERAL DESCRIPTION

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

See outline drawings Nos. 109, 111 and 114 for physical dimensions.

TYPICAL GATE CHARACTERISTICS

Given below are details of a representative function (the MM5611AN)

FEATURES

Wide supply voltage range	3V to 15V
Low power	10nW (typical)
High noise immunity	0.45 V_{DD} (typical)

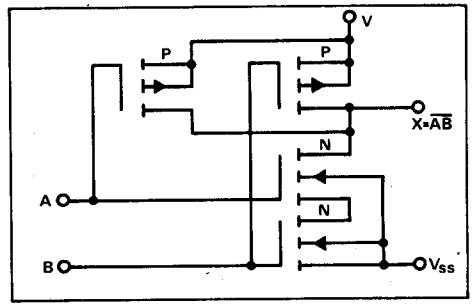
APPLICATIONS

Automotive
Data Terminals
Instrumentation
Medical Electronics
Alarm System
Industrial Controls
Remote Metering
Computers

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin (Note 1)	V_{SS} —0.3V to V_{SS} +15.5V
Operating Temperature Range MM56XXA	—40°C to +85°C
Storage Temperature Range	—65°C to +150°C
Package Dissipation	500mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V

SCHEMATIC DIAGRAM (for a typical NAND gate)



DYNAMIC ELECTRICAL CHARACTERISTICS @T_A = 25°C and C_L = 15pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

Characteristics	Test Conditions V_{DD} (Volts)	Limits Min.	Typ.	Max.	Units
Propagation Delay Time					
Low-to-High Level (t_{PLH})	5	—	50	100	ns
	10	—	25	50	
High-to-Low Level (t_{PHL})	5	—	50	100	ns
	10	—	25	50	
Transition Time					
Low-to-High Level (t_{TLH})	5	—	75	125	ns
	10	—	40	75	
High-to-Low Level (t_{THL})	5	—	75	150	ns
	10	—	50	100	
Input Capacitance (C_I)	Any Input	—	5	—	pF

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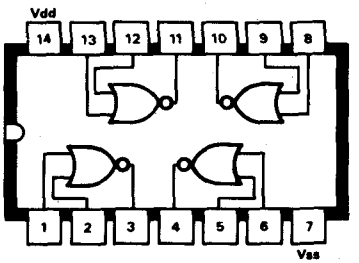
STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions V_O Volts	Test Conditions V_{DD} Volts	Limits −40°C Min	Typ	Max	25°C Min	Typ	Max	85°C Min	Typ	Max	Units
Quiescent Device Current (I_L)		5	—	—	0.5	—	0.005	0.5	—	—	15	μA
		10	—	—	1	—	0.005	1	—	—	30	μA
Quiescent Device Dissipation/Package (P_D)		5	—	—	2.5	—	0.025	10	—	—	75	μW
		10	—	—	10	—	0.05	10	—	—	300	—
Output Voltage Low-Level (V_{OL})		5	—	—	0.01	—	0	0.01	—	—	0.05	V
		10	—	—	0.01	—	0	0.01	—	—	0.05	V
High-Level (V_{OH})		5	4.99	—	—	4.99	5	—	4.95	—	—	V
		10	9.99	—	—	9.99	10	—	9.95	—	—	V
Noise Immunity (All Inputs (V_{NL}))	$V_O \geq 3.5$	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V
	$V_O \geq 7.0$	10	3	—	—	3	4.5	—	2.9	—	—	V
(V_{NH})	$V_O \leq 1.5$	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V
	$V_O \leq 3.0$	10	2.9	—	—	3	4.5	—	3	—	—	V
Output Drive Current N Channel (I_{DN})	0.5	5	0.145	—	—	0.12	0.5	—	0.95	—	—	mA
	0.5	10	0.3	—	—	0.25	0.6	—	0.2	—	—	mA
P Channel (I_{DP})	4.5	5	−0.145	—	—	−0.12	−0.5	—	−0.95	—	—	mA
	9.5	10	−0.35	—	—	−0.3	−1.2	—	−0.24	—	—	mA
Input Current (I_I)			—	—	—	—	10	—	—	—	—	pA

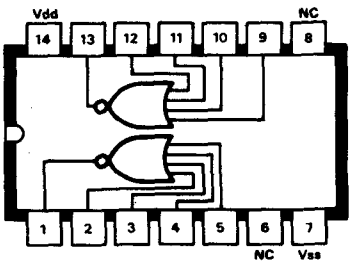
REFERENCE TABLE

Code	Equivalent Designation	Function	Stock No.	Connection Diagram No
MM5601AN	CD4001AN	Quad 2-input NOR Gate	**33119B**	E1
MM5602AN	CD4002AN	Dual 4-input NOR Gate	**33120E**	E2
MM5604AN	CD4004AN	Dual J-K Flip-Flop	**33121C**	E3
MM5609AN	CD4009AN	Hex Inverter Buffer	**33122A**	E4
MM5610AN	CD4010AN	Hex Non-Inverter Buffer	**33123X**	E5
MM5611AN	CD4011AN	Quad 2-Input NAND Gate	**33124H**	E6
MM5612AN	CD4012AN	Dual 4-input NAND Gate	**33125F**	E7
MM5613AN	CD4013AN	Dual 'D' Flip-Flop	**33126D**	E8
MM5614AN	CD4014AN	8 Stage Static Shift Register	**33127B**	E9
MM5616AN	CD4016AN	Quad Bi-Lateral Switch	**33128X**	E10
MM5617AN	CD4017AN	Decade Counter/Divider	**33129R**	E11
MM5619AN	CD4019AN	Quad AND-OR Select Gate	**33130A**	E12
MM5620AN	CD4020AN	14 Stage Ripple-Carry Binary Counter	**34692E**	E17
MM5621AN	CD4021AN	8 Stage Static Shift Register	**33131X**	E13
MM5622AN	CD4022AN	Counter/Divider with 8 Decoded Outputs	**34693C**	E18
MM5623AN	CD4023AN	Triple 3-input NAND Gate	**33132A**	E14
MM5624AN	CD4024AN	Dual J-K Flip Flop	**33133F**	E15
MM5625AN	CD4025AN	Triple 3-input NOR Gate	**34699B**	E19
MM5627AN	CD4027AN	Dual J-K Master/Slave Flip-Flop	**34695X**	E20
MM5630AN	CD4030AN	Quad EXCLUSIVE-OR Gate	**34696H**	E21
MM5635AN	CD4035AN	4-Bit Shift Register	**33134D**	E16
MM5649AN	CD4049AN	Hex Buffer	**34697F**	E22
MM5650AN	CD4050AN	Hex Buffer	**34698D**	E23

E1 **4000AE**
Quad 2-input NOR gate

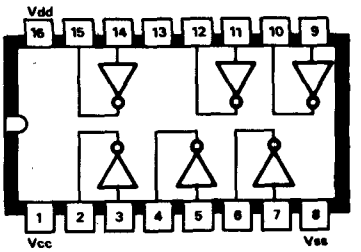


E2 **4002AE**
Dual 4-input NOR gate

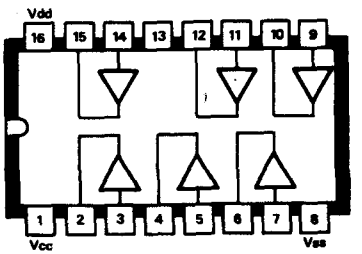


E3 **4004AE**

E4 **4009AE**
Hex buffer (inverting)



E5 **4010AE**
Hex buffer (non-inverting)



E6 **4011AE**
Quad 2-input NAND gate