

# Apple's mobile processors

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## Preface

Apple does not reveal any details about their mobile devices.

There are however [two valuable sources](#) of information relating to Apple's SOC's.

- a) A few companies [teardown](#) electronic devices, such as smartphones, tablets, etc., i.e. they disassembly these products, identify components and functionality, and publish their results either free of charge or for fees, like Chipworks, Techinsights, Ifixit.
- b) In a few cases [even Apple reveals data for optimizing compiler operation](#), as in case of the Cyclone core used in their A7/A8/A8X processors.

The information included in this chapter originates in most parts from these sources.

### Remark

Throughout this chapter the designations of application processor, processor and SOC are used as synonyms.

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# 1. Overview of Apple's mobile processors

# 1. Overview of Apple's mobile processors (1)

## 1. Overview of Apple's mobile processors

### Main features of Apple's early iPhones-1 [4]

	2007	2008	2009	2010
				
	<b>iPhone</b>	<b>iPhone 3G</b>	<b>iPhone 3GS</b>	<b>iPhone 4</b>
<b>Code Name</b>	M68	N82	N88	N90
<b>Model Name</b>	iPhone 1,1	iPhone 1,2	iPhone 2,1	iPhone 3,1
<b>OS</b>	iPhone OS 1.0	iPhone OS 2.0	iPhone OS 3.0	iOS 4
<b>Screen Size</b>	3.5-inch 480x320 at 163ppi	3.5-inch 480x320 at 163ppi	3.5-inch 480x320 at 163ppi	3.5-inch IPS 960x640 at 326ppi
<b>System-on-chip</b>	Samsung S5L8900	Samsung S5L8900	Samsung APL0298C05	Apple A4
<b>CPU</b>	ARM 1176JZ(F)-S	ARM 1176JZ(F)-S	600MHz ARM Cortex A8	800MHz ARM Cortex A8
<b>GPU</b>	Power VR MBX Lite 3D	Power VR MBX Lite 3D	PowerVR SGX535	PowerVR SGX535
<b>RAM</b>	128MB	128MB	256MB	512MB
<b>Storage</b>	4GB/8GB (16GB later)	8GB/16GB	16GB/32GB	16GB/32GB
<b>Rear Camera</b>	2MP	2MP	3MP/480p	5MP/720p, f2.8, 1.75μ
<b>Front Camera</b>	None	None	None	VGA

# 1. Overview of Apple's mobile processors (2)








## Main features of Apple's early iPhones-2 [4]

	2011	2012	2013	2013
				
	<b>iPhone 4S</b>	<b>iPhone 5</b>	<b>iPhone 5c</b>	<b>iPhone 5s</b>
Code Name	N94	N41	N48	N51
Model Name	iPhone 4,1	iPhone 5,1	iPhone 5,3	iPhone 6,1
OS	iOS 5	iOS 6	iOS 7	iOS 7
Screen Size	3.5-inch IPS 960x640 at 326ppi	4-inch 1136x640 in-cell IPS LCD at 326ppi	4-inch 1136x640 in-cell IPS LCD at 326ppi	4-inch 1136x640 in-cell IPS LCD at 326ppi
System-on-chip	Apple A5	Apple A6	Apple A6	64-bit Apple A7, M7 motion c-processor
CPU	800MHz dual-core ARM Cortex A9	1.2GHz dual-core Swift (ARM v7s)	1.2GHz dual-core Swift (ARM v7s)	Swift (ARM v8)
GPU	PowerVR dual-core SGX543MP4	PowerVR triple-core SGX543MP3	PowerVR triple-core SGX543MP3	PowerVR Series 6
RAM	512MB	1GB	1GB	TBD
Storage	16GB/32GB/64GB	16GB/32GB/64GB	16GB/32GB	16GB/32GB/64GB
Rear Camera	8MP/1080p, f2.4, BSI, 1.4 $\mu$	8MP/1080p, f2.4, BSI, 1.4 $\mu$	8MP/1080p, f2.4, BSI, 1.4 $\mu$	8MP/1080p, f2.2, BSI, 1.5 $\mu$
Front Camera	VGA	1.2MP/720p, BSI	1.2MP/720p, BSI	1.2MP/720p, BSI



# 1. Overview of Apple's mobile processors (3)

## Main features of Apple's early iPads -1 [5]

							
	<b>iPad</b>	<b>iPad 2</b>	<b>iPad 3</b>	<b>iPad mini</b>	<b>iPad 4</b>	<b>iPad mini Retina</b>	<b>iPad Air</b>
<b>Code Name</b>	K48	K94	J1, J2	J65		J85	J72
<b>Model Name</b>	iPad 1,1	iPad 2,1	iPad 3,1	iPad 2,5	iPad 3,4		iPad 4,1
<b>OS</b>	iPhone OS 3,2	iOS OS 4,3	iOS 5,1	iOS 6	iOS 6	iOS 7	iOS 7
<b>Screen Size</b>	9.7-inch IPS LED 1024x768 @ 132 ppi	9.7-inch IPS LED 1024x768 @ 132 ppi	9.7-inch IPS LED 2048x1536 @ 264 ppi	7.9-inch IPS LED 1024x768 @ 163 ppi	9.7-inch IPS LED 2048x1536 @ 264 ppi	7.9-inch IPS LED 2048x1536 @ 326 ppi	9.7-inch IPS LED 2048x1536 @ 264 ppi
<b>System-on-chip</b>	Apple A4	Apple A5	Apple A5X	Apple A5	Apple A6X	64-bit Apple A7, M7 motion c-processor	64-bit Apple A7, M7 motion c-processor
<b>CPU</b>	800MHz ARM Cortex A8	1GHz dual-core ARM Cortex A9	1GHz dual-core ARM Cortex A9	1GHz dual-core ARM Cortex A9	1.4GHz dual-core Swift ARM v7s	Dual-core Cyclone (ARM v8)	Dual-core Cyclone (ARM v8)
<b>GPU</b>	PowerVR SGX535	PowerVR dual-core SGX543MP2	PowerVR quad-core SGX543MP4	PowerVR dual-core SGX543MP2	PowerVR quad-core SGX554MP4	PowerVR Series 6	PowerVR Series 6
<b>Coprocessor</b>	None	None	None	None	None	M7 Motion	M7 Motion
<b>RAM</b>	256MB	512MB	1GB	512MB	1GB	TBD	TBD
<b>Storage</b>	16GB/32GB/64GB	16GB/32GB/64GB	16GB/32GB/64GB	16GB/32GB/64GB	16GB/32GB/64GB/ 128GB	16GB/32GB/64GB/ 128GB	16GB/32GB/64GB/ 128GB
<b>Top Data Speed</b>	HSPA	HSPA	LTE	LTE	LTE	LTE	LTE
<b>SIM</b>	Micro	Micro	Micro	Nano	Micro	Nano	Nano
<b>Rear Camera</b>	None	1.3mo/720p	5mp, 1080p	5mp, 1080p	5mp, 1080p	5mp, 1080p	5mp, 1080p
<b>Front Camera</b>	None	0.3mp/VGA	0.3pm/VGA	1.2mp, 720p	1.2mp, 720p	1.2mp, 720p	1.2mp, 720p
<b>Bluetooth</b>	Bluetooth 2.1 + EDR	Bluetooth 2.1 + EDR	Bluetooth 4.0	Bluetooth 4.0	Bluetooth 4.0	Bluetooth 4.0	Bluetooth 4.0
<b>WiFi</b>	802.11 a/b/g/n	802.11 a/b/g/n	802.11 a/b/g/n	802.11 a/b/g/n	802.11 a/b/g/n	802.11 a/b/g/n MIMO	802.11 a/b/g/n MIMO
<b>GPS</b>	aGPS	aGPS	aGPS, GLONASS	aGPS, GLONASS	aGPS, GLONASS	aGPS, GLONASS	aGPS, GLONASS
<b>Sensors</b>	Accelerometer, proximity, compass	Accelerometer, proximity, compass, gyroscope	Accelerometer, proximity, compass, gyroscope	Accelerometer, proximity, compass, gyroscope	Accelerometer, proximity, compass, gyroscope	Accelerometer, proximity, compass, gyroscope	Accelerometer, proximity, compass, gyroscope
<b>Speakers</b>	Mono	Mono	Mono	Stereo	Mono	Stereo	Stereo
<b>Connector</b>	30-pin Dock	30-pin Dock	30-pin Dock	Lightning	Lightning	Lightning	Lightning
<b>Size</b>	9.56x7.47x0.53	9.5x7.31x0.34 inches	9.5x7.31x0.37 inches	7.87x5.3x0.28 inches	9.5x7.31x0.37 inches	7.87x5.3x0.29 inches	9.4x6.6x0.29 inches
<b>Weight</b>	1.5 lbs	1.33 lbs	1.44 lbs	0.68 lbs	1.44 lbs	0.73 lbs	1 lbs
<b>Battery</b>	25 watt hour	25 watt hour	42.5 watt hour	16.3 watt hour	42.5 watt hour	23.8 watt hour	32.4 watt hour
<b>Colors</b>	Black	Black/White	Black/White	Slate/Silver	Black/White	Space gray/Silver	Space gray/Silver
<b>Price</b>	Wi-Fi \$499, \$599, \$699, Data \$629, \$729, \$829	Wi-Fi \$499, \$599, \$699, Data \$629, \$729, \$829	Wi-Fi \$499, \$599, \$699, Data \$629, \$729, \$829	Wi-Fi \$329, \$429, \$529, Data \$459, \$559, \$659	Wi-Fi \$499, \$599, \$699, Data \$629, \$729, \$829	Wi-Fi \$399, \$499, \$599, \$699, Data \$529, \$629, \$729, \$829	Wi-Fi \$499, \$599, \$699, \$799 Data \$629, \$729, \$829, \$929
<b>Release Date</b>	2010-04-03	2011-03-11	2012-03-16	2012-11-02	2012-11-02	2013-11	2013-11-01

# 1. Overview of Apple's mobile processors (4)




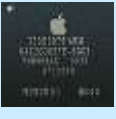

## Main features of Apple's early iPads -2 [6]



	Air	Air 2	Mini	Mini 2	Mini 3
Price	Starts at £319 (Wi-Fi) Starts at £419 (Wi-Fi + Cellular)	Starts at £399 (Wi-Fi) Starts at £499 (Wi-Fi + Cellular)	Starts at £199 (Wi-Fi) Starts at £299 (Wi-Fi + Cellular)	Starts at £239 (Wi-Fi) Starts at £339 (Wi-Fi + Cellular)	Starts at £319 (Wi-Fi) Starts at £419 (Wi-Fi + Cellular)
Display	9.7-inch Retina 2048x1536 res 264 ppi	9.7-inch Retina 2048x1536 res 264 ppi	7.9-inch 1024x768 res 163 ppi	7.9-inch Retina 2048x1536 res 326 ppi	7.9-inch Retina 2048x1536 res 326 ppi
Wi-Fi Capacity	16GB, 32GB	16GB, 64GB, 128GB	16GB	16GB, 32GB	16GB, 64GB, 128GB
Wi-Fi + Cellular Capacity	16GB, 32GB	16GB, 64GB, 128GB	16GB	16GB, 32GB	16GB, 64GB, 128GB
Preinstalled Apple SIM	No	Yes (Wi-Fi + Cellular)	No	No	Yes (Wi-Fi + Cellular)
Processor	A7 chip with 64-bit architecture, M7 motion coprocessor	A8X chip with 64-bit architecture, M8 motion coprocessor	A5 Chip	A7 chip with 64-bit architecture, M7 motion coprocessor	A7 chip with 64-bit architecture, M7 motion coprocessor







# 1. Overview of Apple's mobile processors (5)

## Main features of Apple's 32-bit application processors used in their mobiles (1)

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
	S5L8900X		90 nm	72 mm <sup>2</sup>	1x ARM1176 412 MHz	ARMv6	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103 MHz	128 MB 16-bit SCh LPDDR-266 (532 MB/sec)	6/2007 6/2008	<ul style="list-style-type: none"> <li>• iPhone (2G)</li> <li>• iPod Touch (1st gen.)</li> <li>• iPhone 3G</li> </ul>
	APL0278 or S5L8720		65 nm	36 mm <sup>2</sup>	1x ARM1176 412–533 MHz	ARMv6	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103–133 MHz	32/128 MB 32-bit SCh LPDDR-133	9/2008	<ul style="list-style-type: none"> <li>• iPod Touch (2nd gen.)</li> <li>• iPod Nano (4th gen.)</li> </ul>
	APL0298 or S5L8920		65 nm	71.8 mm <sup>2</sup>	1x Cortex-A8 600 MHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 150 MHz (1.2 GFLOPS)	256 MB 32-bit SCh LPDDR-400 (1.6 GB/sec)	6/2009	• iPhone 3GS
	APL2298 or S5L8922		45 nm	41.6 mm <sup>2</sup>	1x Cortex-A8 600–800 MHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 150–200 MHz (1.2–1.6 GFLOPS)	256 MB 32-bit SCh LPDDR-400 (1.6 GB/sec)	9/2009	• iPod Touch (3rd gen.)
<b>A4</b>	APL0398 or S5L8930		45 nm	53.3 mm <sup>2</sup>	1x Cortex-A8 0.8–1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 512 KB	PowerVR SGX535 @ 200–250 MHz (1.6–2 GFLOPS)	256 MB (iPad) 512 MB (iPhone 4) 32-bit DCh LPDDR-400 (3.2 GB/sec)	3/2010	<ul style="list-style-type: none"> <li>• iPad (1st gen.)</li> <li>• iPhone 4</li> <li>• iPod Touch (4th gen.)</li> <li>• Apple TV (2nd gen.)</li> </ul>

# 1. Overview of Apple's mobile processors (6)







## Main features of Apple's 32-bit application processors used in their mobiles (2)

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A5</b>	APL0498 or S5L8940		45 nm	122.2 mm <sup>2</sup>	2x Cortex-A9 0.8–1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP2 (2C) @ 200–250 MHz (12.8–16 GFLOPS)	512 MB 32-bit DCh LPDDR2-800 (6.4 GB/sec)	3/2011	• iPad 2 • iPhone 4S
	APL2498 or S5L8942		32 nm HKMG	69.6 mm <sup>2</sup>	2x Cortex-A9 0.8–1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP2 (2C) @ 200–250 MHz (12.8–16 GFLOPS)	512 MB 32-bit DCh LPDDR2-800 (6.4 GB/sec)	3/2012	• iPad 2 (iPad 2,4) • iPod Touch (5th gen.) • iPad Mini
	APL7498 or S5L8947		32 nm HKMG	37.8 mm <sup>2</sup>	1x Cortex-A9 1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP2 (2C) @ 200–250 MHz (12.8–16 GFLOPS)	512 MB 32-bit DCh LPDDR2-800 (6.4 GB/sec)	3/2013	• AppleTV 3 (AppleTV3,2)
<b>A5X</b>	APL5498 or S5L8945		45 nm	165 mm <sup>2</sup>	2x Cortex-A9 1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP4 (4C) @ 250 MHz (32 GFLOPS)	1 GB 32-bit 4Ch LPDDR2-800 (12.8 GB/sec)	3/2012	• iPad (3rd gen.)
<b>A6</b>	APL0598 or S5L8950		32 nm HKMG	96.7 mm <sup>2</sup>	2x Swift 1.3 GHz	ARMv7s	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP3 (3C) @ 266 MHz (25.5 GFLOPS)	1 GB 32-bit DCh LPDDR2-1066 (8.528 GB/sec)	9/2012	• iPhone 5 • iPhone 5C
<b>A6X</b>	APL5598 or S5L8955		32 nm HKMG	123 mm <sup>2</sup>	2x Swift 1.4 GHz	ARMv7s	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX554MP4 (4C) @ 266 MHz (68.1 GFLOPS)	1 GB 32-bit 4Ch LPDDR2-1066 (17.1 GB/sec)	10/2012	• iPad (4th gen.)



# 1. Overview of Apple's mobile processors (7)






## Main features of Apple's 64-bit application processors used in their mobiles (1)

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A7</b>	APL0698 or S5L8960		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.3 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB LS: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2013	iPhone 5S iPad Mini 2 iPad Mini 3
	APL5698 or S5L8965		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB LS: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	10/2013	iPad Air 9.7"
<b>A8</b>	APL1011		20 nm HKMG	89 mm <sup>2</sup>	2x Typhoon 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB LS: 4 MB	PowerVR GX6450 (4C) @ 450 MHz (115.2 GFLOPS)	1GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2014	iPhone 6 iPhone 6 Plus
<b>A8X</b>	APL1012		20 nm HKMG	128 mm <sup>2</sup>	3xTyphoon 1.5 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 2 MB LS: 4 MB	PowerVR GX6850 (5C) @ 450 MHz (230.4 GFLOPS)	2 GB 64-bit DCh LPDDR3-1600 (25.6 GB/sec)	10/2014	iPad Air 2 9.7"
<b>A9</b>	APL1022 (TSMC) APL0898 (Samsung)		16 nm FinFET 14 nm FinFET	104.5 mm <sup>2</sup>	2xTwister 1.85 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 (6C) @ 450 MHz (172.8 GFLOPS)	2 GB 64-bit SCh LPDDR4-3200 (25.6 GB/sec)	9/2015	iPhone 6s iPhone 6s Plus iPhone SE
<b>A9X</b>	APL1021 (TSMC)		16 nm FinFET	147 mm <sup>2</sup>	2xTwister 2.16-2.26 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: none	PowerVR 7XT series (12C) @ n.a. MHz (345.6 GFLOPS)	2 GB/4 GB 64-bit DCh LPDDR4-3200 (51.2 GB/sec)	11/2015	iPad Pro 9.7" iPad Pro 12.9"

LS: System cache, it services the entire SoC

# 1. Overview of Apple's mobile processors (8)

## Main features of Apple's 64-bit application processors used in their mobiles (2)

Appl. proc.S	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache (big core)	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A10 (Fusion)</b>	APL1W24		16 nm FinFET	125 mm <sup>2</sup>	2xHurricane (2.34 GHz)+ 2x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 Plus (6C) @ >650 MHz (>250 GFLOPS) (redesigned)	2 GB/3 GB LPDDR4	9/2016	iPhone 7 iPhone 7 Plus
<b>A10X (Fusion)</b>	APL1071 (TSMC)		10 nm FinFET	96.4 mm <sup>2</sup>	3xHurricane (2.38 GHz)+ 3x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: none	PowerVR GT7600 Plus (12C)	3 GB/4 GB LPDDR4	6/2017	iPad Pro 10.5" iPad Pro 12.9" Apple TV 4K
<b>A11 Bionic</b>	APL1W72 (TSMC)		10 nm FinFET	88 mm <sup>2</sup>	2x Monsoon (2.39 GHz) + 4x Mistral (1.42 GHz)z	ARM V8.2-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: 4 MB	Apple Custom GPU (3C)	2 GB/3 GB? LPDDR4X	9/2017	iPhone 8 iPhone 8 Plus iPhone X
<b>A12 Bionic</b>	APL1W82 (TSMC)		7 nm FinFET	83 mm <sup>2</sup>	2x Vortex (2.50 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	3 GB/4 GB LPDDR4X	9/2018	iPhone XS 5.8" iPhone XS Max iPhone XR 6.1"
<b>A12X Bionic</b>	APL1083 (TSMC)		7 nm FinFET	122 mm <sup>2</sup>	4x Vortex (2.48 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	6 GB LPDDR4X	10/2018	iPad Pro 11" iPad Pro 12.9"

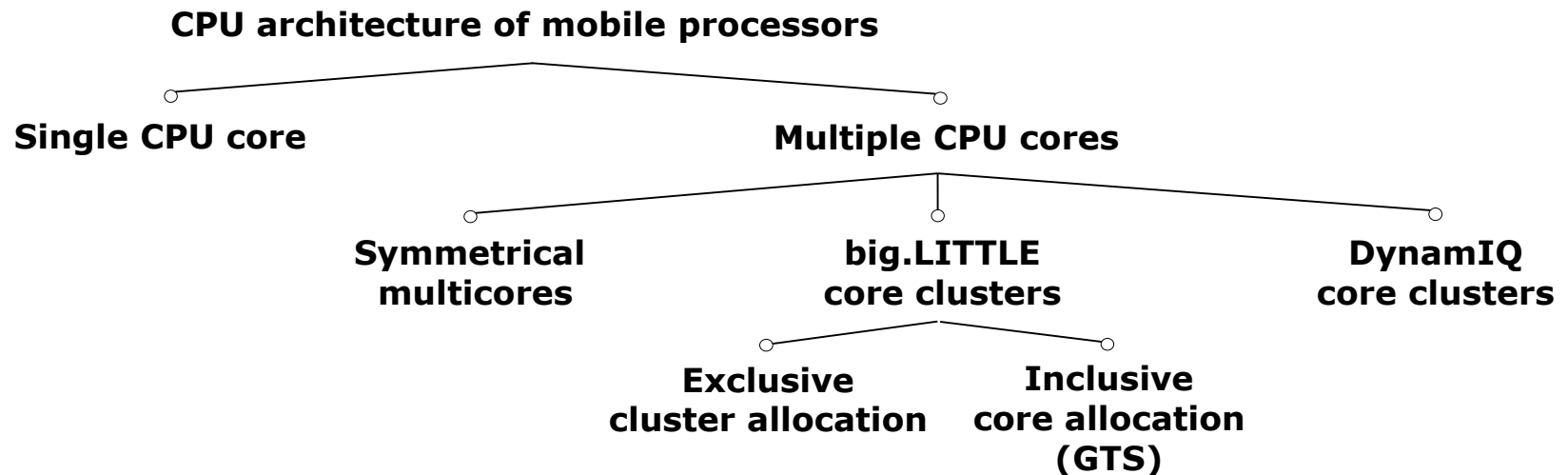
LS: System cache, it services the entire SoC

## 1. Overview of Apple's mobile processors (9)

**Note** that the X-taged processors, like A6X, A8X, A9X are primarily targeting tablets, whereas those without the X tag are primarily smartphones.

# 1. Overview of Apple's mobile processors (10)

## Evolution of CPU architectures in Apple's mobiles



Apple ARM1176 (2007) until A4 (2010) → A5 (2011) (2C) → A10 (2016) (2+2) → A11 (2017) (2+4)

Samsung Exynos 3110 (2010) → 3250 2C (2011) 4412 4C (2012) → 5410 (2013) (4+4) → 5420 (2013) (4+4) → 9810 (2018) (4+4)

Qualcomm Snapdragon MSM 7225 (2007) → 8260 2C (2013) 400 4C (2013) → 808 (2+4) (2014) 810 (4+4) (2015) → 845 (2018) (4+4)





Huawei Kirin (K3V1) (2009) → (K3V2 (2012)) → 920 (4+4) (2014)

MediaTek MT6218B (2003) → MT6582 4C (2013) MT6592 8C (2013) → MT6595 8C (2014)



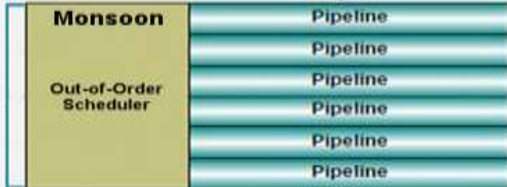
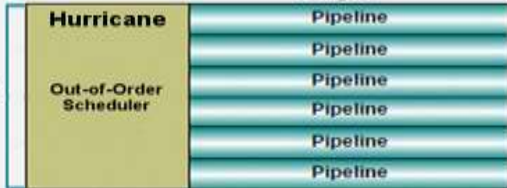
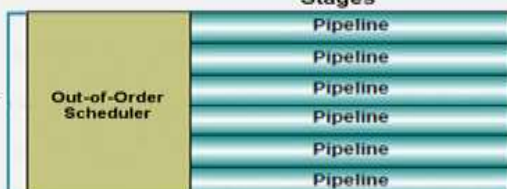
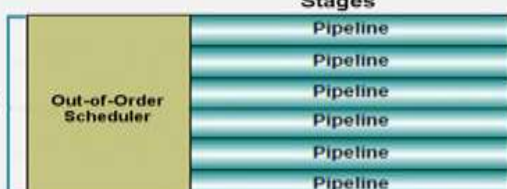
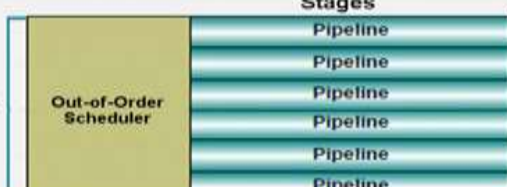
# 1. Overview of Apple's mobile processors (11)

Key features of Apple's 32-bit application processors (based on [2]) -1

2012	Apple Swift (A6)	3-wide (32-bit)	3 decode		2 cores	1.3 GHz
2011	ARM Cortex-A9 (A5)	2-wide (32-bit)	2 decode		2 cores	0.8-1.0 GHz
2009	ARM Cortex-A8 (A4)	2-wide (32-bit)	2 decode		1 core	600-1000 MHz
2007	ARM 1176	1-wide (32-bit)	1 decode		1 core	412-533 MHz

# 1. Overview of Apple's mobile processors (12)

Key features of Apple's 64-bit application processors (based on [2]) -1

2017	<b>Bionic (A11)</b>	<b>6-wide (64-bit)</b>	6 decode	 <p><b>Monsoon</b> Out-of-Order Scheduler</p> <p>Stages Pipeline Pipeline Pipeline Pipeline Pipeline</p>	<b>2 big cores (Monsoon) + 4 LITTLE cores (Mistral)</b>	<b>2.39 GHz/ 1.42 GHz</b>
2016	<b>Fusion (A10/A10X)</b>	<b>6-wide (64-bit)</b>	6 decode	 <p><b>Hurricane</b> Out-of-Order Scheduler</p> <p>Stages Pipeline Pipeline Pipeline Pipeline Pipeline</p>	<b>2-3 big cores (Hurricane) + 2-3 LITTLE cores (Zephyr)</b>	<b>2.33 GHz/ 1.1 GHz</b>
2015	<b>Apple Twister (A9/A9X)</b>	<b>6-wide (64-bit)</b>	6 decode	 <p>Out-of-Order Scheduler</p> <p>Stages Pipeline Pipeline Pipeline Pipeline Pipeline</p>	<b>2 cores</b>	<b>1.85- 2.26 GHz</b>
2014	<b>Apple Typhoon (A8/A8X)</b>	<b>6-wide (64-bit)</b>	6 decode	 <p>Out-of-Order Scheduler</p> <p>Stages Pipeline Pipeline Pipeline Pipeline Pipeline</p>	<b>2-3 cores</b>	<b>1.4-1.5 GHz</b>
2013	<b>Apple Cyclone (A7)</b>	<b>6-wide (64-bit)</b>	6 decode	 <p>Out-of-Order Scheduler</p> <p>Stages Pipeline Pipeline Pipeline Pipeline Pipeline</p>	<b>2 cores</b>	<b>1.3-1.4 GHz</b>

# 1. Overview of Apple's mobile processors (13)

## Width of mobile cores

### Width of mobile cores (or of big cores of big.LITTLE or dynamIQ core clusters)

2-wide

3-wide

4-wide

6-wide

ARM	v7 ISA based (32-bit) Cortex-A cores except the Cortex-A15) (2005-2009)	→	v7 ISA based (32-bit) Cortex-A15 (2010)
	v8 ISA-based Cortex-A73 (2016)	→	v8 ISA-based (64-bit) Cortex-A line, except the Cortex-A73 (2012-)
Intel	Atom family (2008-2016)		
AMD	Cat family (2011-2015)		

Apple	Cortex-A8 (2009)	→	A6 (Swift (2012)	→	A7 (Cyclone (2013) and subsequent cores
Qualcomm	Scorpion v7 ISA (S1-S3) (2007-2010)	→	Krait v7 ISA (S4/S400/S60x/S80x) (2012-2014)		
			Kryo/Kryo 280 v8 ISA (S820/821/835) (2015/2016/2017)		
			Kryo 385 v8.2 ISA (S845) (2018)		
Samsung		→	Exynos 5 v7 ISA (2013-2014)	→	M1 core v8 ISA (2016) (Exynos 8 Octa)
		→	/Exynos 7 v8 ISA (2016)	→	M2 core v8 ISA (2017) (Exynos 9 Octa)
				→	M3 core v8.2 ISA (2018) (Exynos 9810)

# 1. Overview of Apple's mobile processors (14)

## Remark

Certain early mobile processors are only 1-wide, like

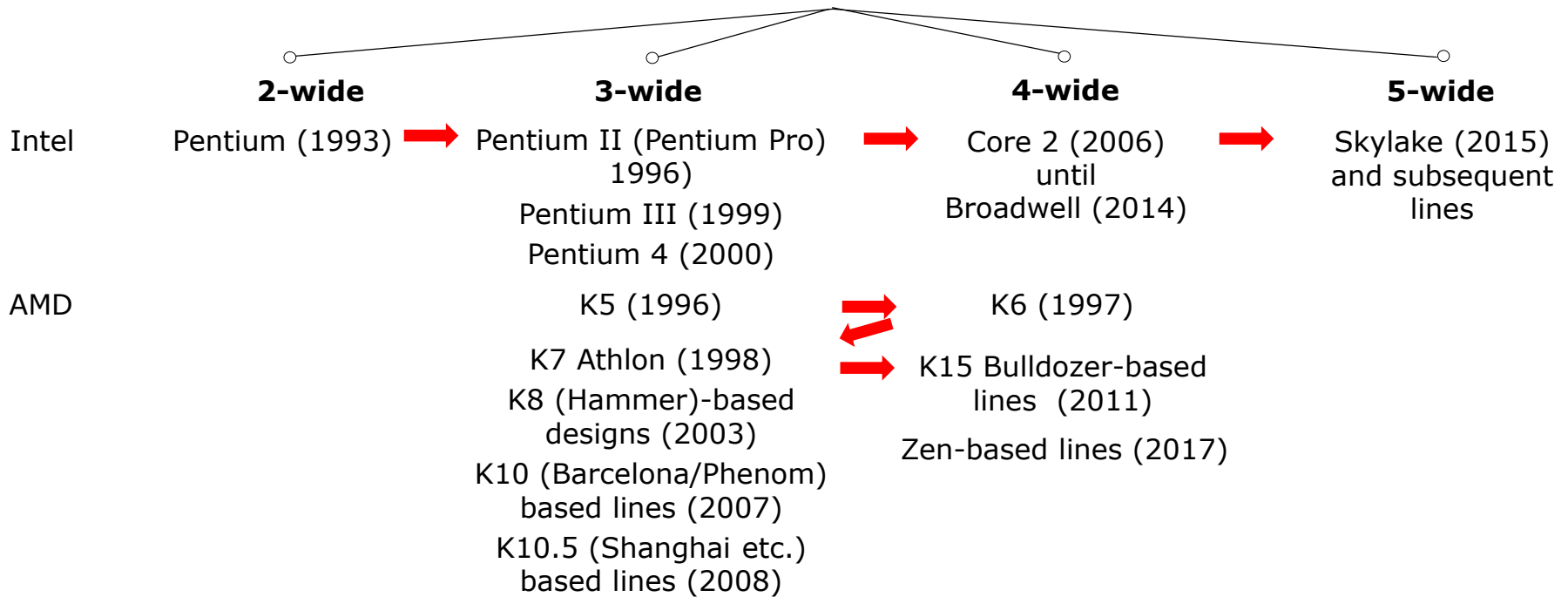
- ARM's 1176 used in Apple's iPhone (2007) or
- ARM's Cortex-A5 (2009)

nevertheless, in the previous slide these processors are not indicated for better visibility of the entire Figure.

# 1. Overview of Apple's mobile processors (15)

For comparison: Width of Intel's and AMD's basic microarchitectures

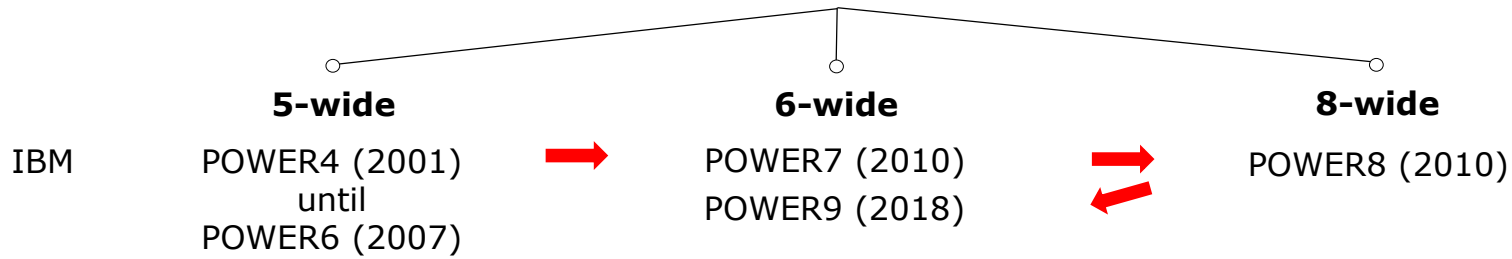
## Width of Intel's and AMD's basic microarchitectures



# 1. Overview of Apple's mobile processors (16)

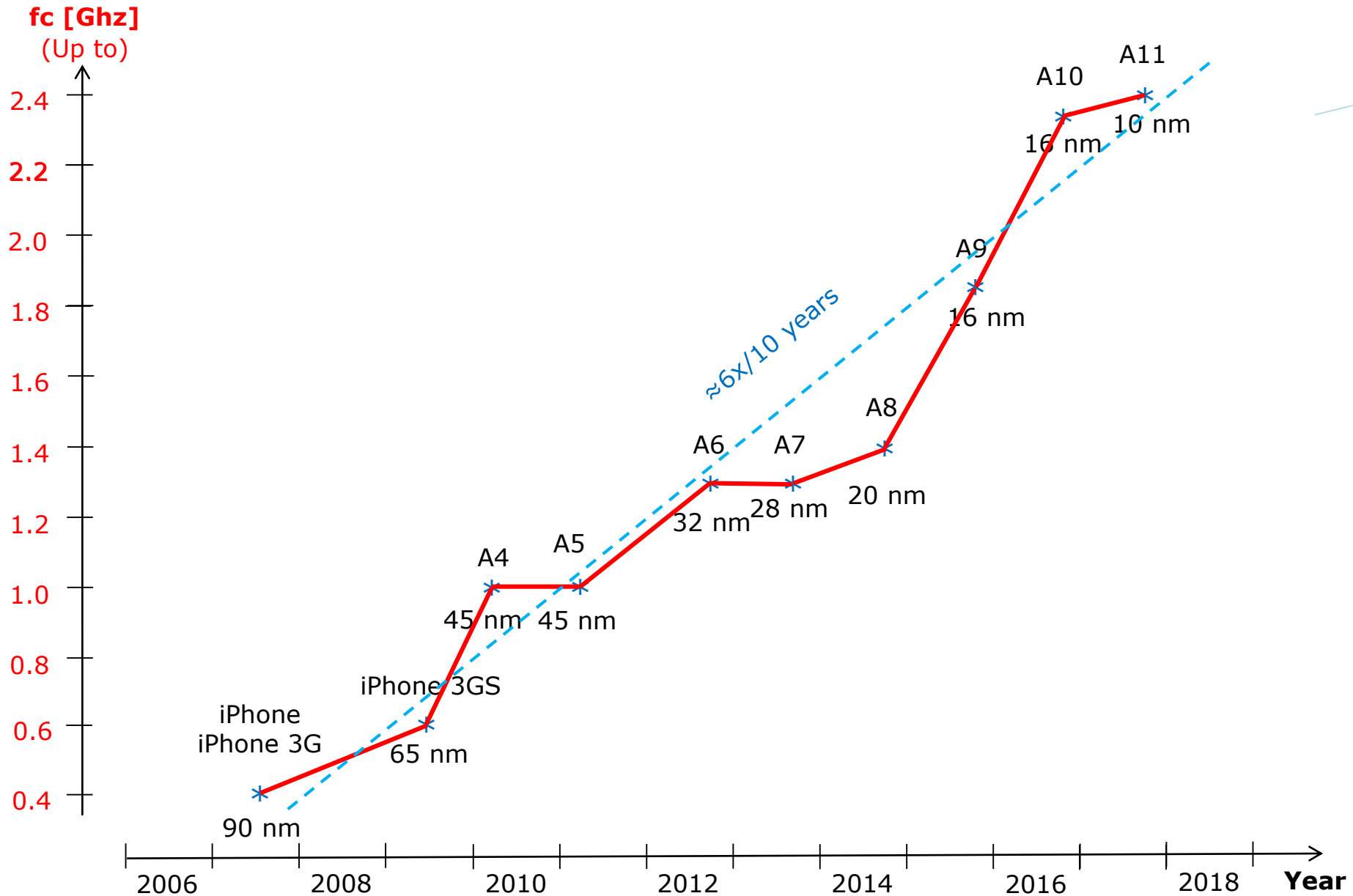
For comparison: Width of IBM's POWER microarchitectures

## Width of IBM's POWER microarchitectures



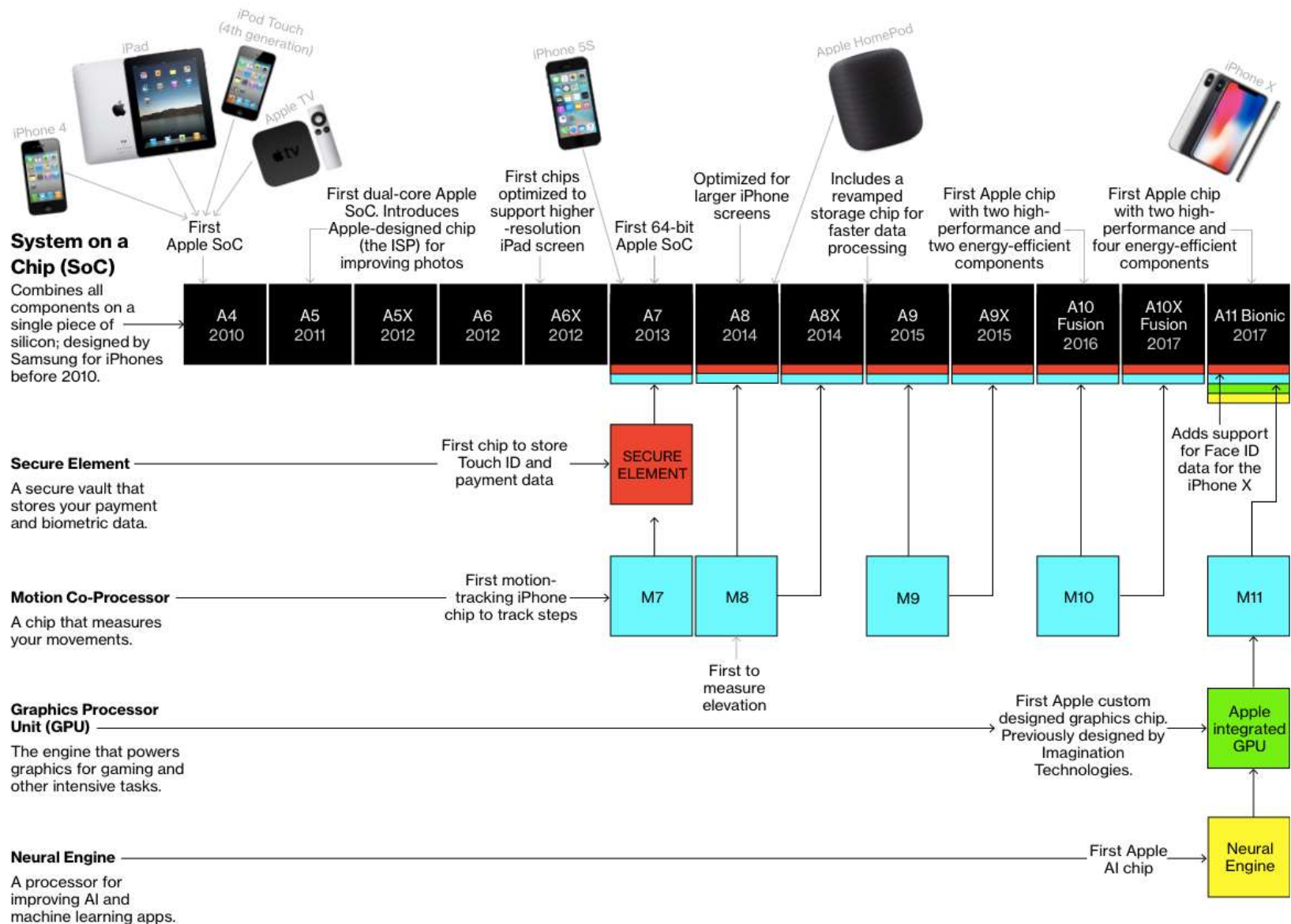
# 1. Overview of Apple's mobile processors (17)

Increasing the clock frequency in Apple's mobiles [40]



# 1. Overview of Apple's mobile processors (18)

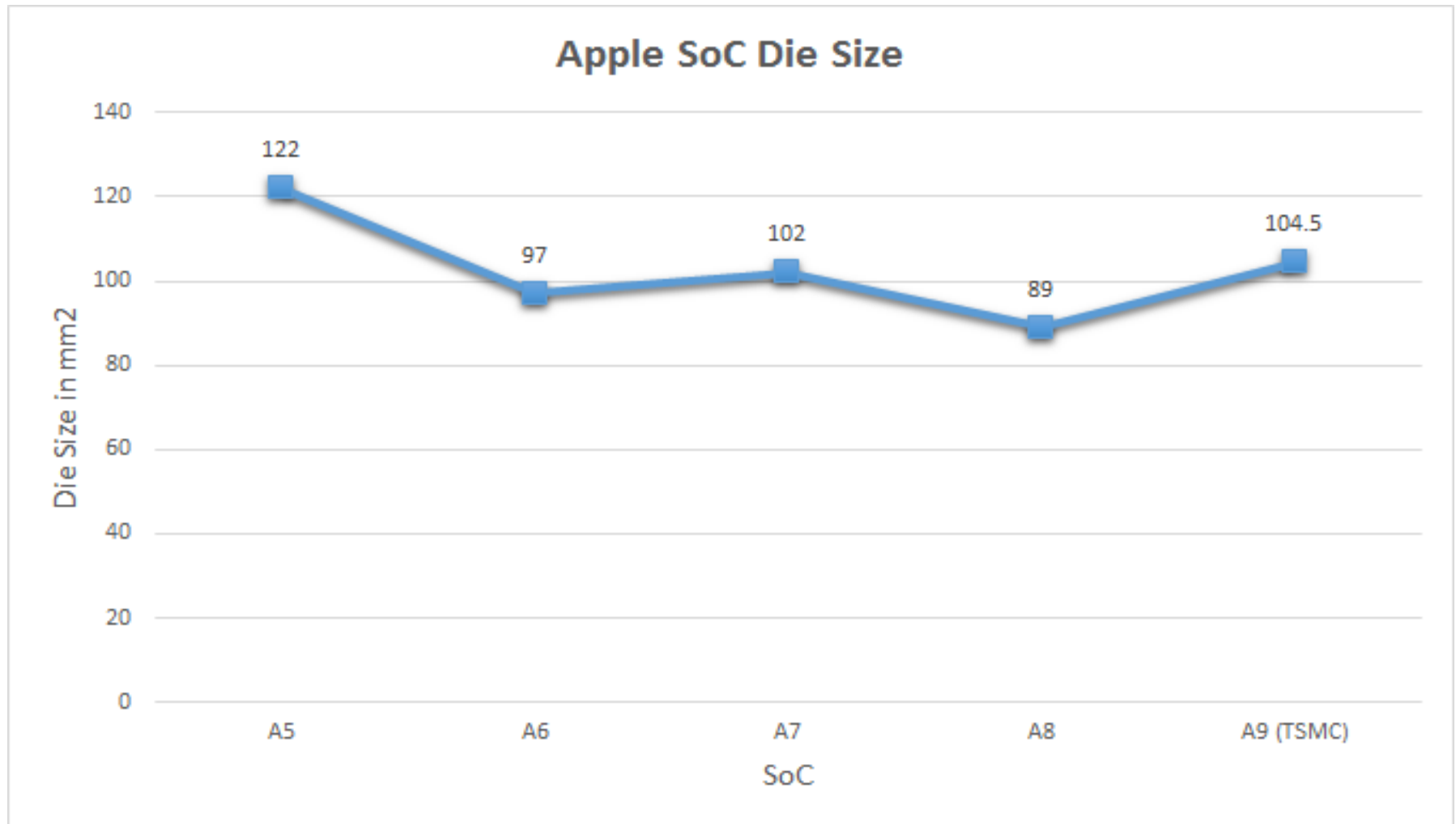
## New features and accelerators in Apple's processors [48]





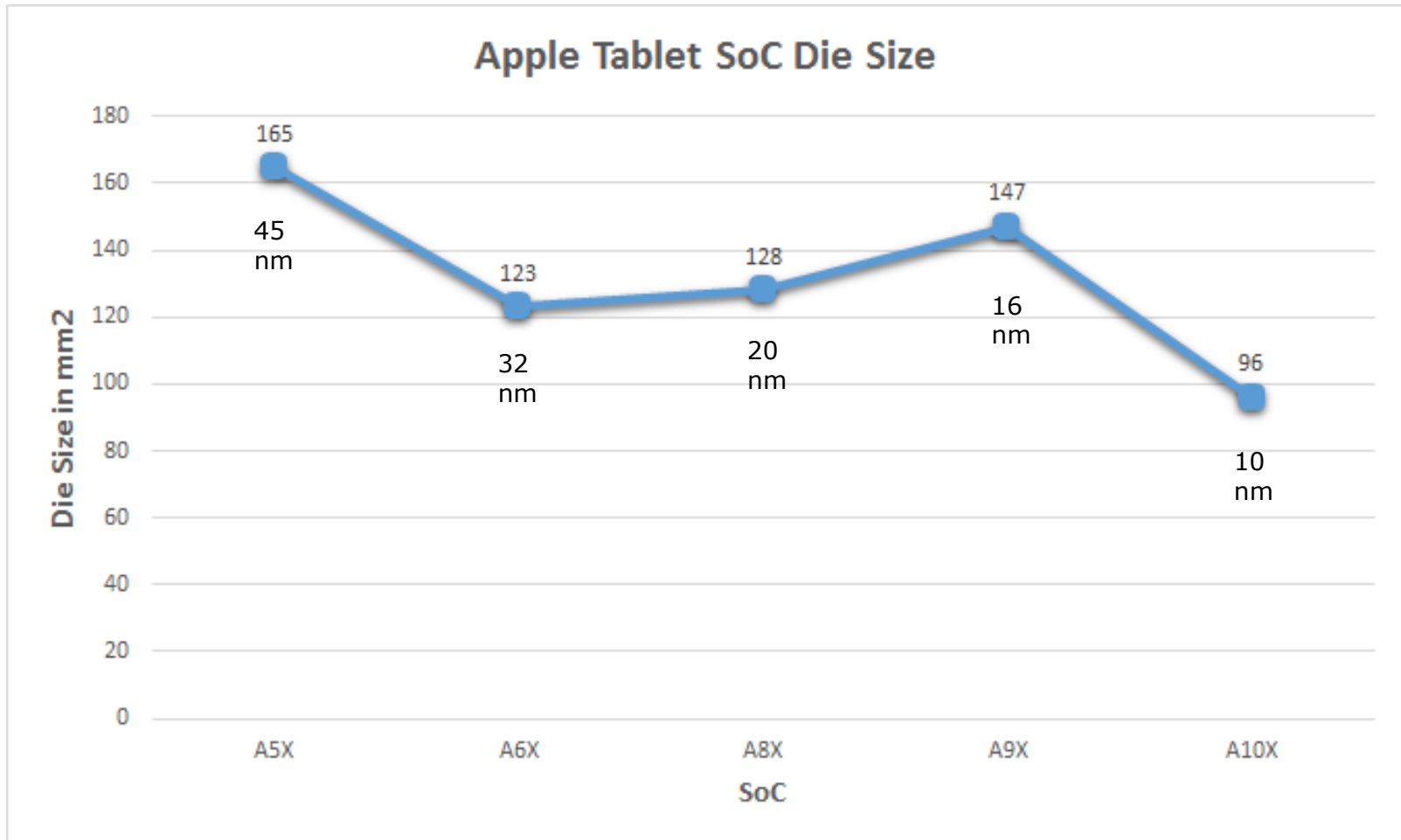
# 1. Overview of Apple's mobile processors (19)

Die sizes of Apple's A5 to A9 mobile SoCs [40]



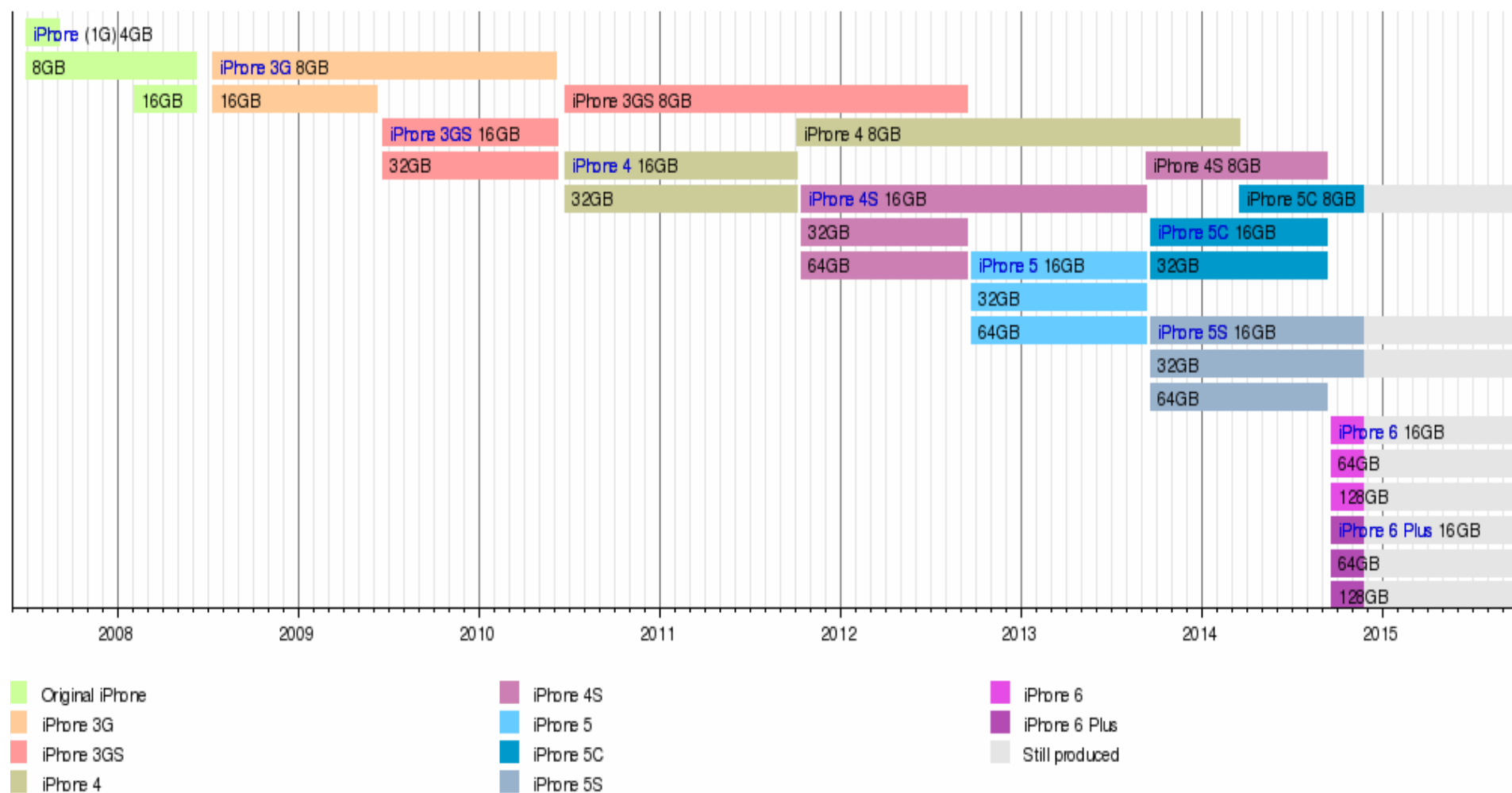
## 1. Overview of Apple's mobile processors (20)

Die sizes of Apple's A5X to A10X tablet SoCs [49]



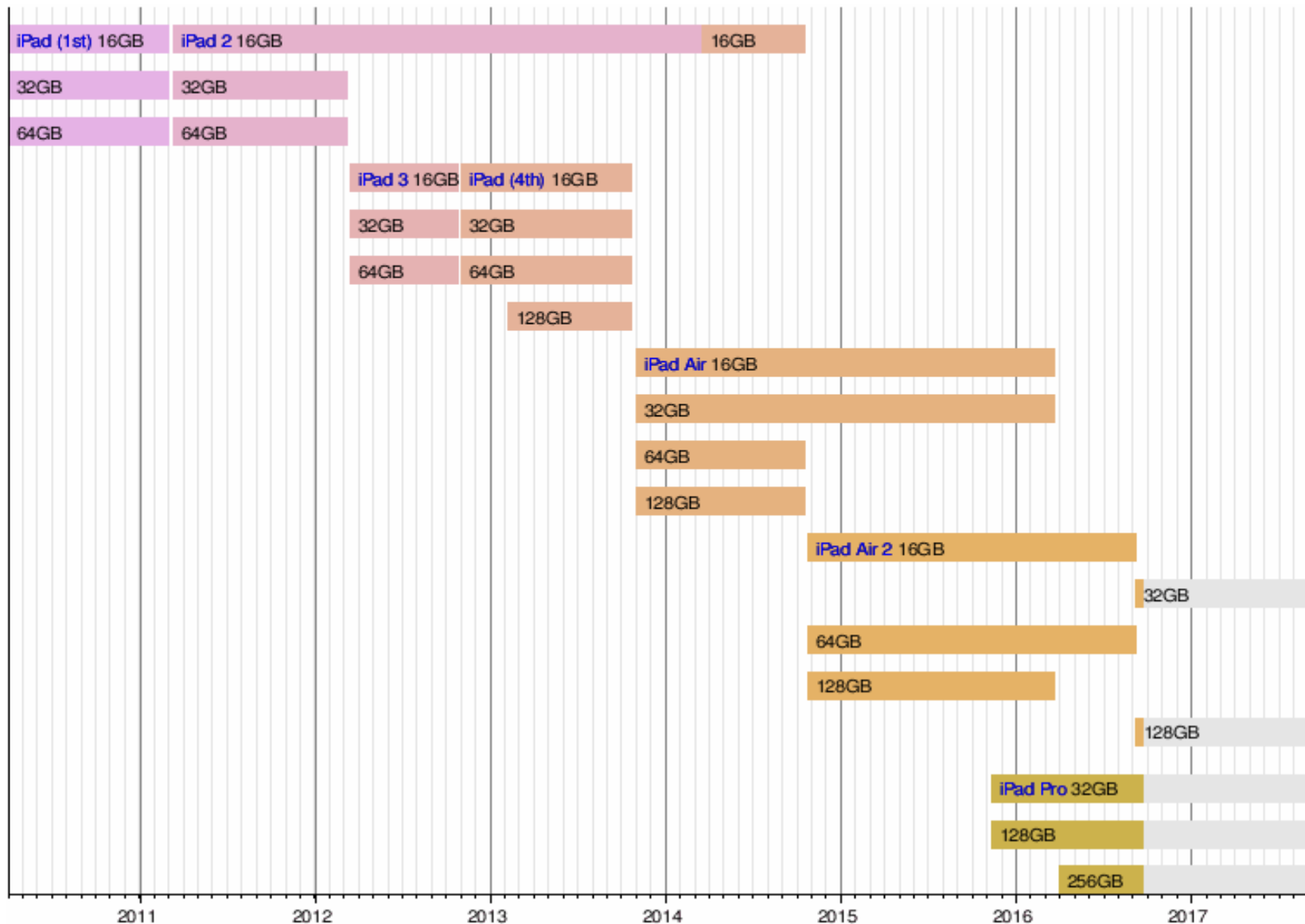
# 1. Overview of Apple's mobile processors (21)

## Overview of flash memory sizes in Apple's iPhones [3]



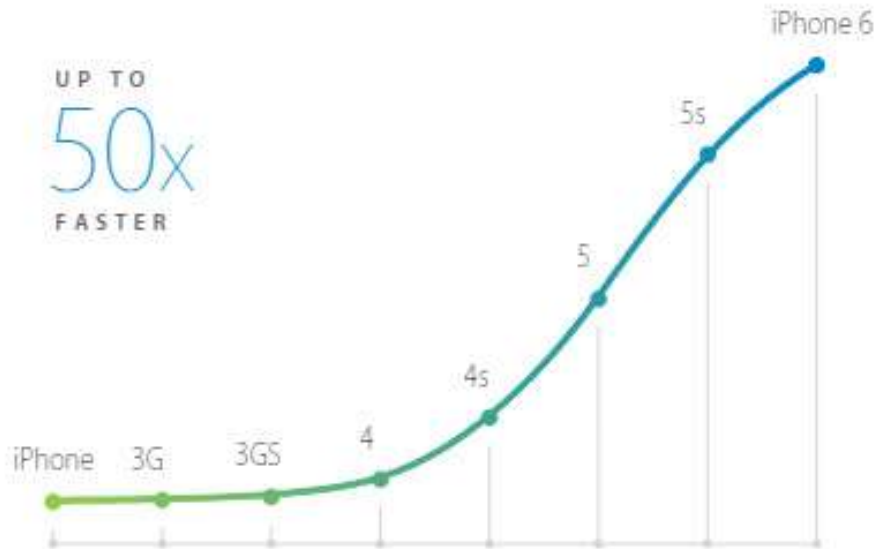
# 1. Overview of Apple's mobile processors (22)

## Overview of flash memory sizes in Apple's iPads [46]

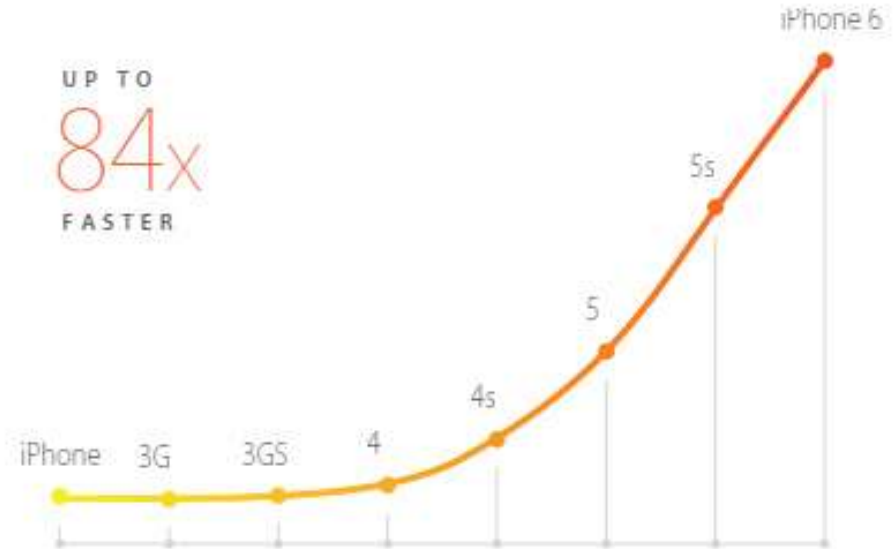


# 1. Overview of Apple's mobile processors (23)

## Performance increase of Apple's iPhones (Up to the iPhone 6) [7]



CPU PERFORMANCE

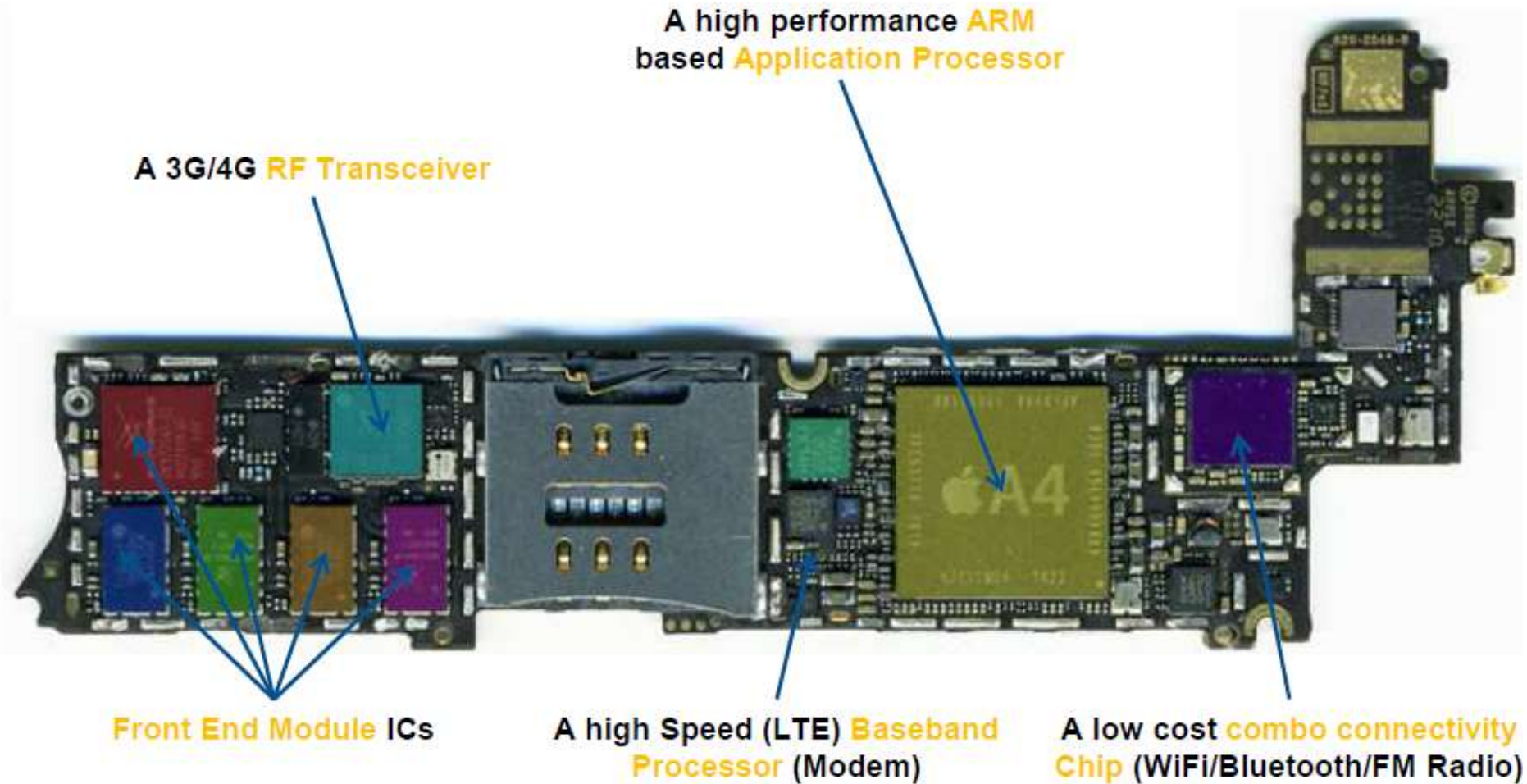


GPU PERFORMANCE

iPhone 6 A8 SoC CPU and GPU performance graph (Apple's own figures)

# 1. Overview of Apple's mobile processors (24)

Main components of a smartphone or tablet [9]



## Note

Processor memory (usually implemented as stacked memory on the processor) and flash memory (usually implemented as an individual chip) not indicated in the Figure.

# 1. Overview of Apple's mobile processors (25)

## Apple's patent asset [10]

- ◆ A quick look at Apple's 13,000 patents broken down by issue date and type/origin – shows a healthy purchasing of legacy patents, and aggressive pursuit of design patents which they have used successfully in litigations
- ◆ Major recent increase in total # of patents issued yearly indicates Apple's strategic decision to pursue many patents regarding their product releases since 2003

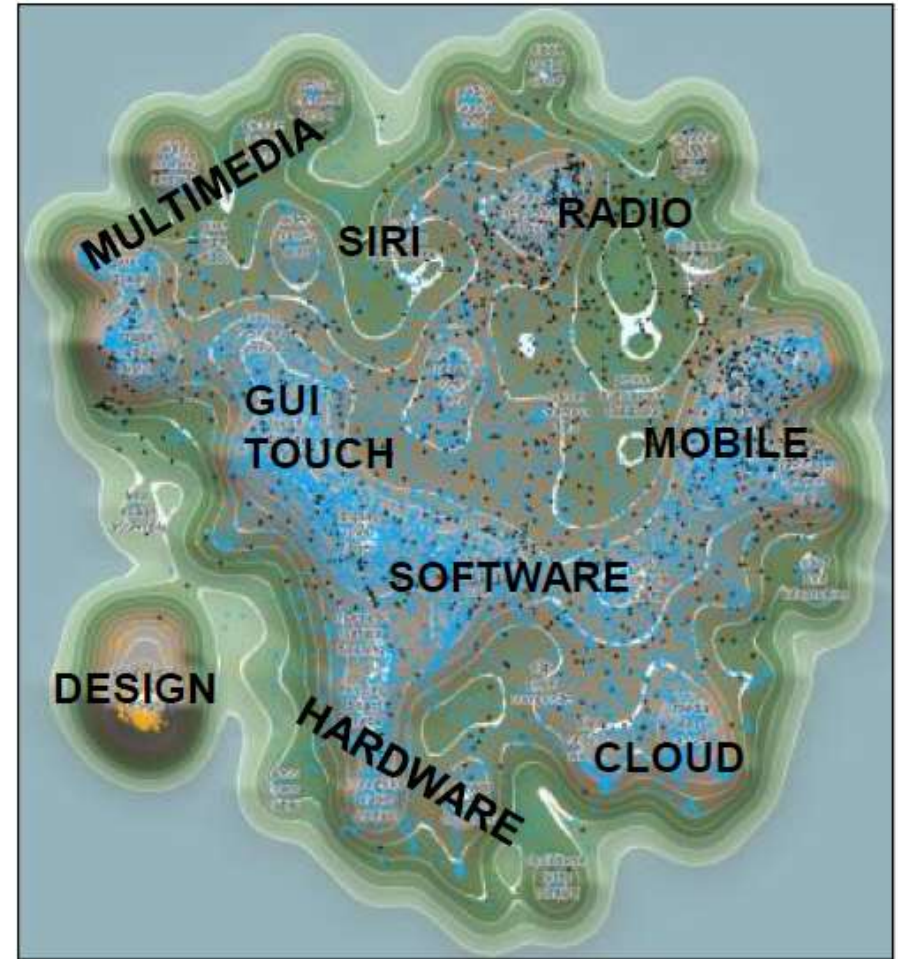
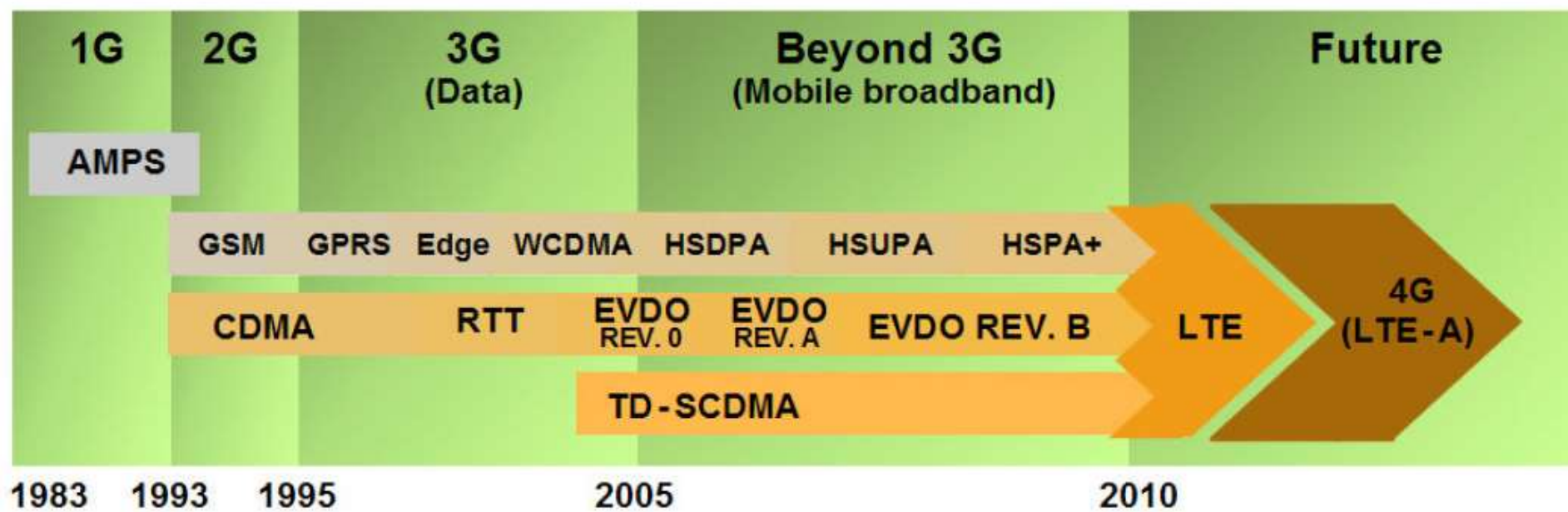


Figure: Granted Apple patents sorted by technology [10]



# 1. Overview of Apple's mobile processors (26)

Evolution of cellular standards – until 2010 [8]





## 2. Apple's original iPhone

## 2. Apple's original iPhone (1)

### 2. Apple's original iPhone

Designated also as the **iPhone 2G**.

Introduced in **1/2007** by Steve Jobs at the MacWorld Expo.








Figure: Steve Jobs introducing the iPhone at MacWorld Expo in 1/2007 [11]

The iPhone became available in 6/2007 in the US and later elsewhere.

## 2. Apple's original iPhone (2)

### Main features of the original iPhone

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
	S5L8900X		90 nm	72 mm <sup>2</sup>	1x ARM1176 412 MHz	ARMv6	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103 MHz	128 MB 16-bit SCh LPDDR-266 (532 MB/sec)	6/2007 6/2007	<ul style="list-style-type: none"> <li>• iPhone (2G)</li> <li>• iPod Touch (1st gen.)</li> <li>• iPhone 3G</li> </ul>
	APL0278 or S5L8720		65 nm	36 mm <sup>2</sup>	1x ARM1176 412–533 MHz	ARMv6	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103–133 MHz	32/128 MB 32-bit SCh LPDDR-133	9/2008	<ul style="list-style-type: none"> <li>• iPod Touch (2nd gen.)</li> <li>• iPod Nano (4th gen.)</li> </ul>
	APL0298 or S5L8920		65 nm	71.8 mm <sup>2</sup>	1x Cortex-A8 600 MHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 150 MHz (1.2 GFLOPS)	256 MB 32-bit SCh LPDDR-400 (1.6 GB/sec)	6/2009	• iPhone 3GS
	APL2298 or S5L8922		45 nm	41.6 mm <sup>2</sup>	1x Cortex-A8 600–800 MHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 150–200 MHz (1.2–1.6 GFLOPS)	256 MB 32-bit SCh LPDDR-400 (1.6 GB/sec)	9/2009	• iPod Touch (3rd gen.)
<b>A4</b>	APL0398 or S5L8930		45 nm	53.3 mm <sup>2</sup>	1x Cortex-A8 0.8–1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 512 KB	PowerVR SGX535 @ 200–250 MHz (1.6–2 GFLOPS)	256 MB (iPad) 512 MB (iPhone 4) 32-bit DCh LPDDR-400 (3.2 GB/sec)	3/2010	<ul style="list-style-type: none"> <li>• iPad (1st gen.)</li> <li>• iPhone 4</li> <li>• iPod Touch (4th gen.)</li> <li>• Apple TV (2nd gen.)</li> </ul>

## 2. Apple's original iPhone (3)

### Implementation of the iPhone (termed also as the iPhone 2)

The original iPhone was based on a **PoP package** (Package on Package), designated as S5L8900B01, that included **3 dies**:

- the **SOC die** with the **ARM1176ZF-S 32-bit processor** (executing the ARMv6 ISA) and Imagination Technologies' **PowerVR MBX Lite 3D graphics accelerator**, and
- **two 512 Mb LPDDR-266 SDRAM dies** (providing 128 MB stacked memory),

as illustrated below.

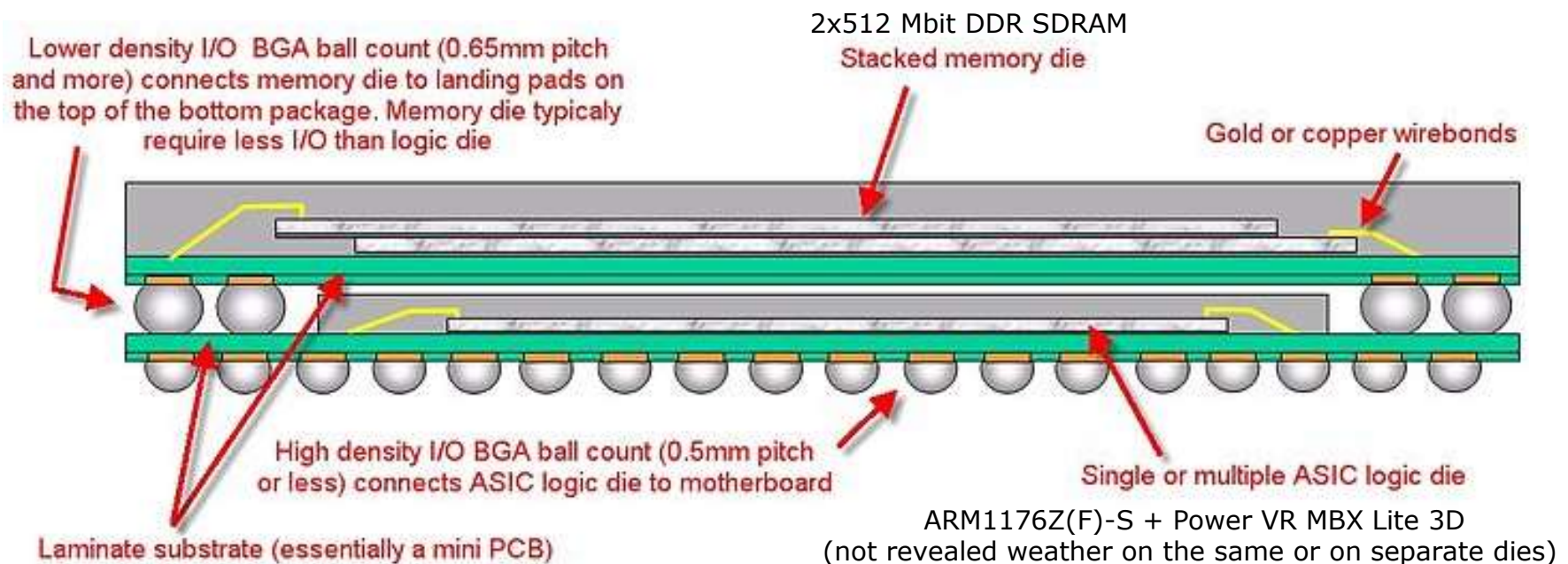
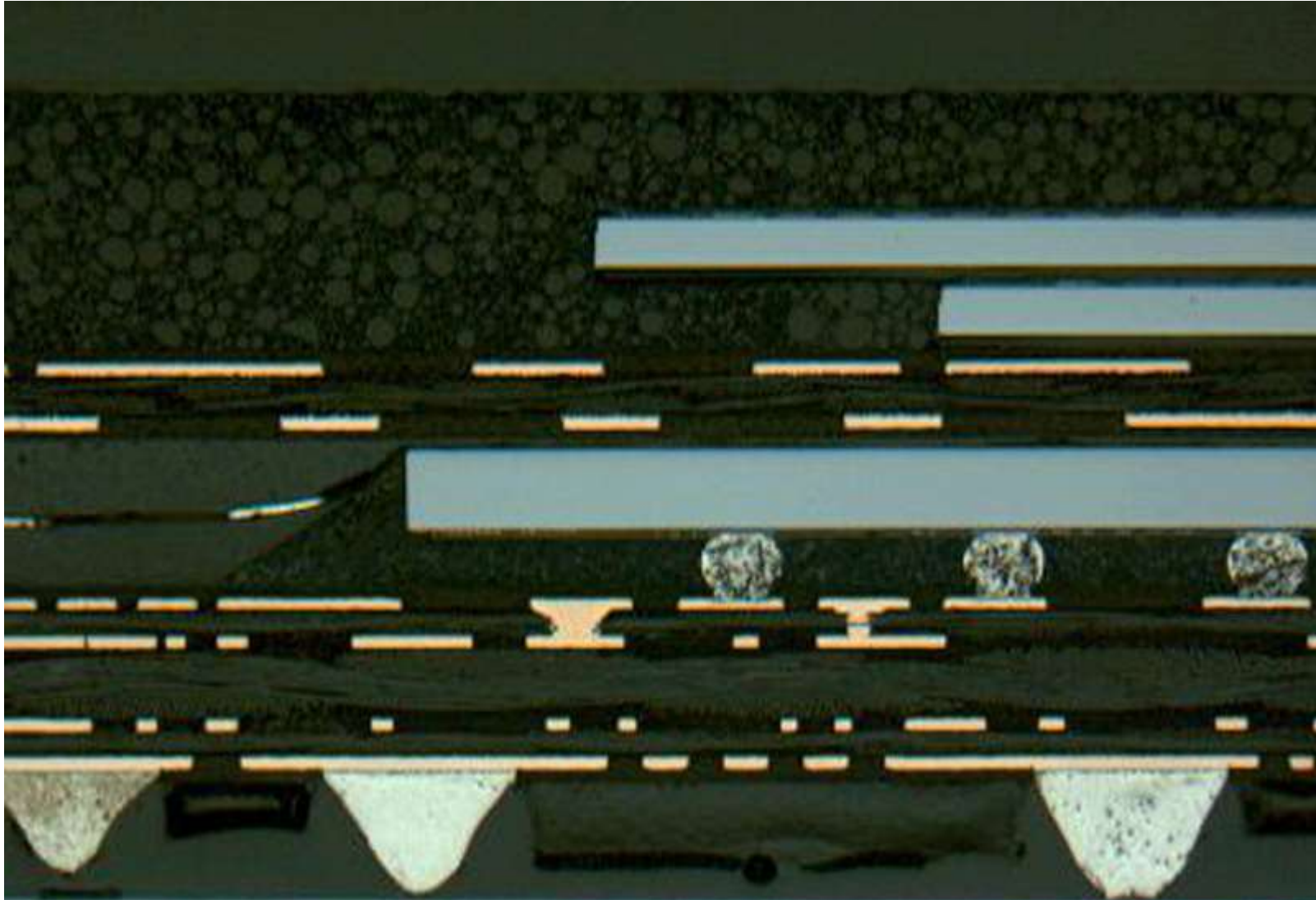


Figure: iPhone's heart, the S5L8900B01 PoP, fabricated by Samsung (90 nm) [4]

## 2. Apple's original iPhone (4)

Cross section of the iPhone [12]



**DRAM dies**

**SOC die**

**Solder balls**

**Mini PCB**

## 2. Apple's original iPhone (5)

### Remarks

- PoPs are fabricated as Multi-Chip Packages (MCPs).
- MCP became standardized by JEDEC about 2006 (JC-63).
- First PoPs emerged in cell phones around 2004 [13].
- First generation PoP technology typically integrates the baseband or application processor with one or two memory dies, as indicated in the next Figure.



Figure: Possible PoP structure for implementing a baseband or application processor and two memory dies [13]

- According to this, using PoP packaging for integrating the application processor and the memory in Apple's original iPhone was an early advanced packaging solution.



## 2. Apple's original iPhone (6)

### The ARM1176JZF-S CPU [14]

- The 32-bit CPU runs at a lower clock rate (412 MHz) than possible (667 MHz) to save power.
- It supports the ARMv6 ISA.
- It is a single issue processor.
- It has 16 kB instruction and 16 kB data caches, but no L2 cache.
- It has a Vector FP Processing Unit (VFP).

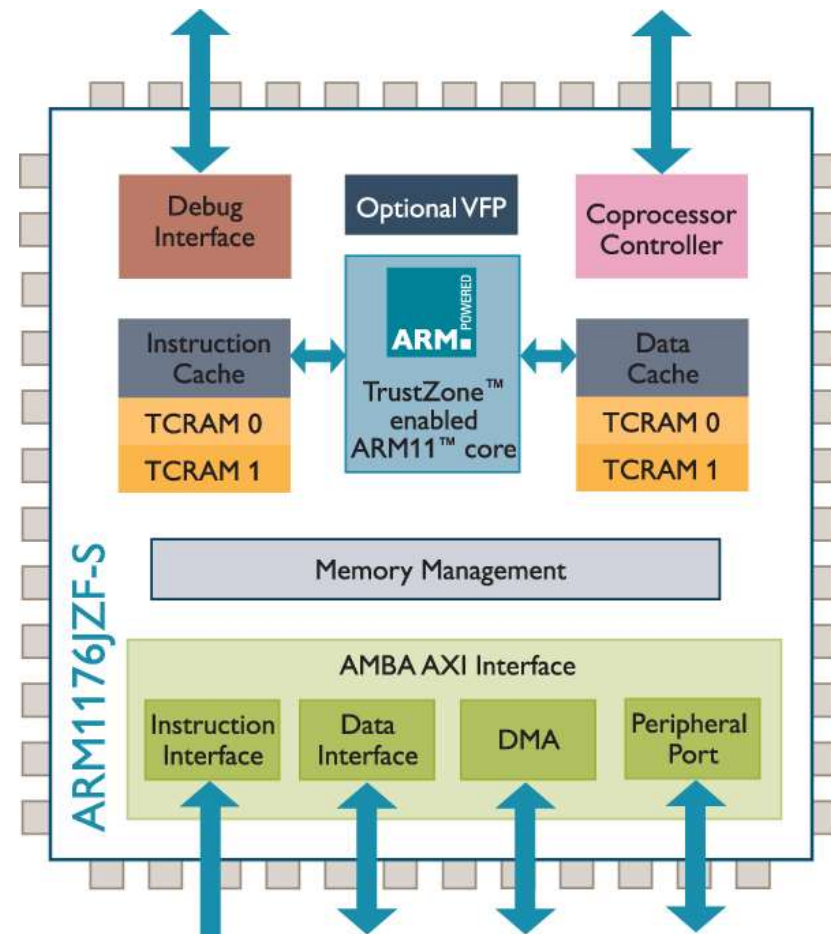


Figure: The ARM1176JZF-S CPU [14]

## 2. Apple's original iPhone (7)

The PowerVR MBX Lite 3D graphics accelerator

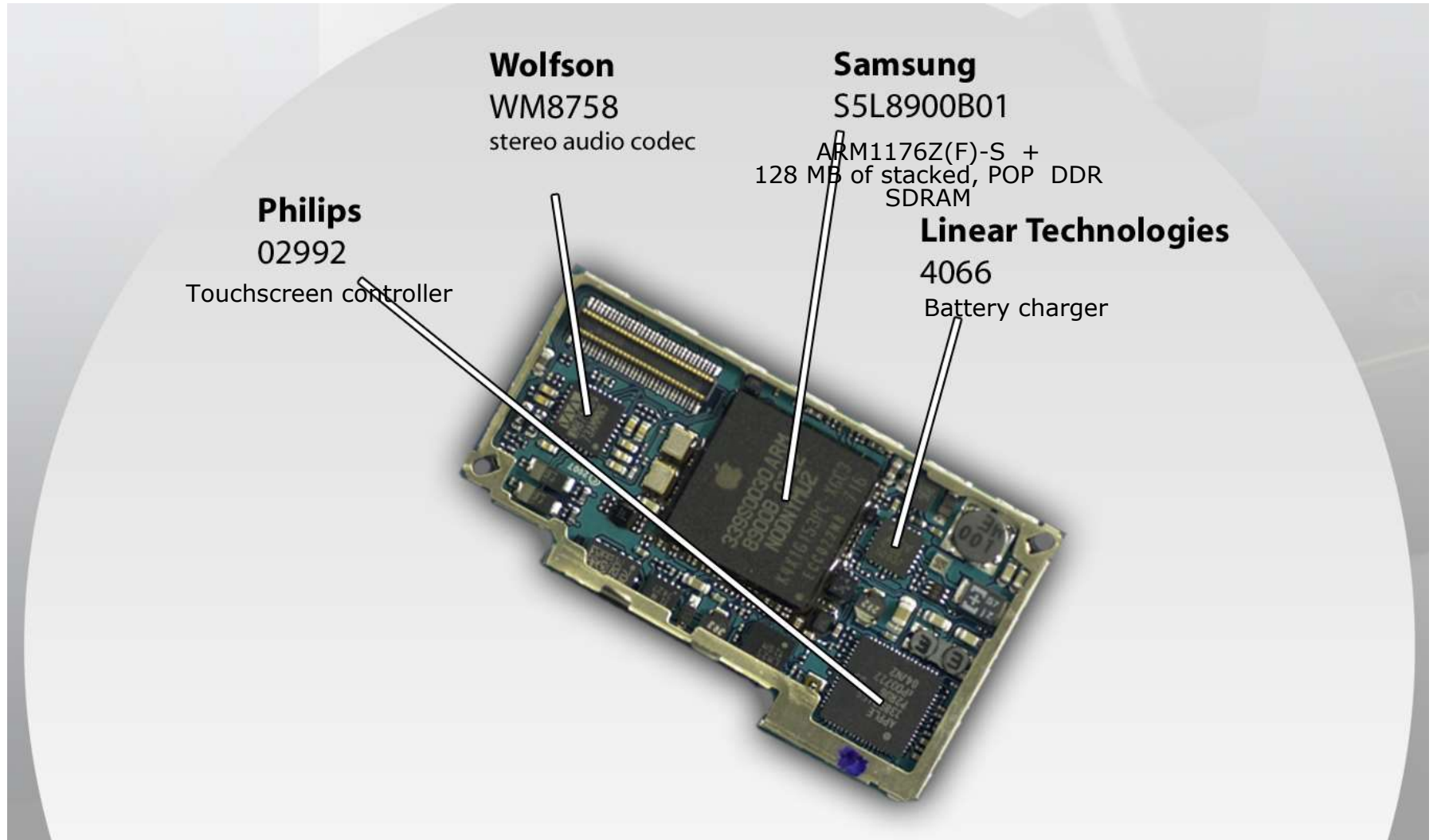
PowerVR branding	Architecture Generation	Example Application	Approximate date of introduction
PowerVR1	Series1	Matrox m3D, Compaq Presario video cards	1998
PowerVR2	Series2	Sega Dreamcast, Neon250 PC video cards	1998
PowerVR3	Series3	KYRO PC video cards	2001
PowerVR4	Series4	STM STG5000 chip for PC video cards	Unreleased
PowerVR MBX		iPhone, iPhone 3G, iPod touch	2004
PowerVR SGX	Series5	Palm Pre, iPhone 3GS	2009

Figure: Generations of PowerVR graphics IPs (from Imagination Technologies) [15]



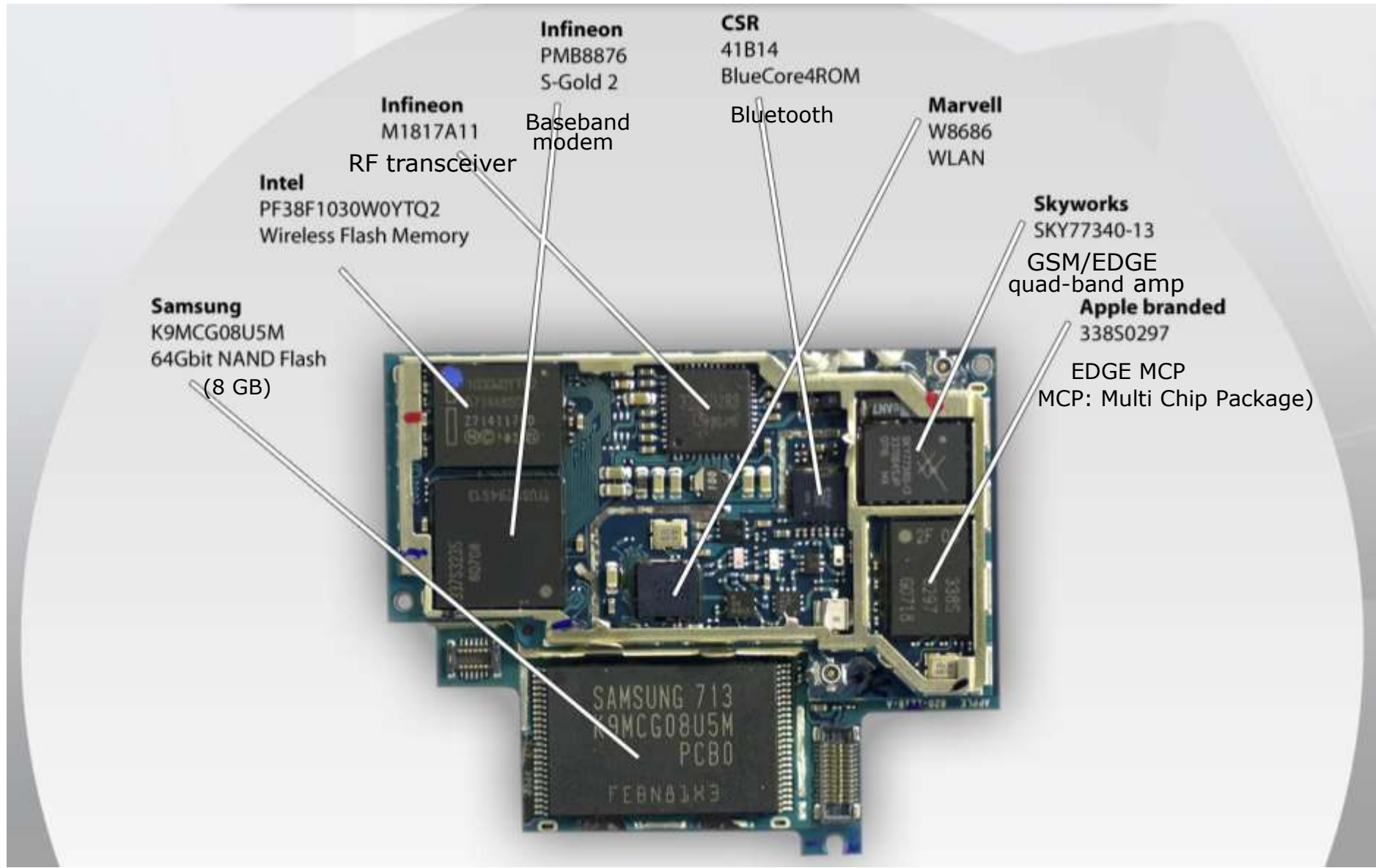
## 2. Apple's original iPhone (8)

### The iPhone board (one side) [16]



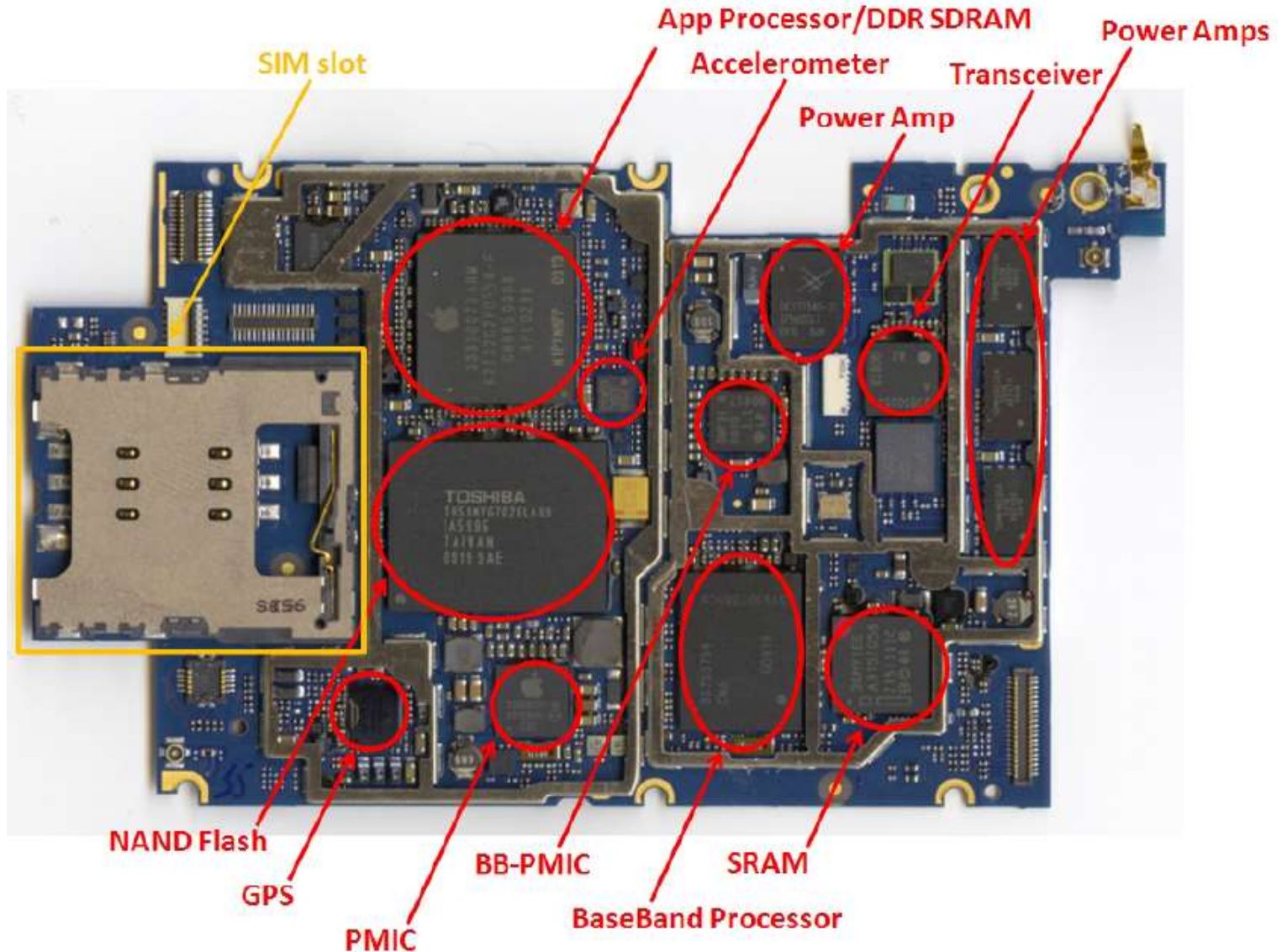
## 2. Apple's original iPhone (9)

### The iPhone board (the other side) [16]



## 2. Apple's original iPhone (10)

Apple iPhone 3GS board [47]






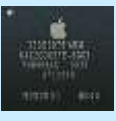

### 3. Apple A4

### 3. Apple A4

- Introduced in particular in the
  - iPad (2010) and
  - iPhone 4 (2010).
- The **A4** processor is **Apple's first in-house design** done in cooperation with Intrinsity (a fabless semiconductor company, acquired by Apple in 2010).
- With Intrinsity an experienced team of chip designers, specialized in high speed physical design joined Apple.
- Intrinsity just finalized tuning Samsung's Hummingbird CPU for high speed and low power, in cooperation with Samsung.
- Apple's A4 is allegedly based on the Hummingbird core.

### 3. Apple A4 (2)

#### Main features of the A4

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
	S5L8900X		90 nm	72 mm <sup>2</sup>	1x ARM1176 412 MHz	ARMv6	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103 MHz	128 MB 16-bit Sch LPDDR-266 (532 MB/sec)	6/2007 6/2007	<ul style="list-style-type: none"> <li>• iPhone (2G)</li> <li>• iPod Touch (1st gen.)</li> <li>• iPhone 3G</li> </ul>
	APL0278 or S5L8720		65 nm	36 mm <sup>2</sup>	1x ARM1176 412–533 MHz	ARMv6	L1i: 16 KB L1d: 16 KB	PowerVR MBX Lite @ 103–133 MHz	32/128 MB 32-bit Sch LPDDR-133	9/2008	<ul style="list-style-type: none"> <li>• iPod Touch (2nd gen.)</li> <li>• iPod Nano (4th gen.)</li> </ul>
	APL0298 or S5L8920		65 nm	71.8 mm <sup>2</sup>	1x Cortex-A8 600 MHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 150 MHz (1.2 GFLOPS)	256 MB 32-bit Sch LPDDR-400 (1.6 GB/sec)	6/2009	• iPhone 3GS
	APL2298 or S5L8922		45 nm	41.6 mm <sup>2</sup>	1x Cortex-A8 600–800 MHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 256 KB	PowerVR SGX535 @ 150–200 MHz (1.2–1.6 GFLOPS)	256 MB 32-bit Sch LPDDR-400 (1.6 GB/sec)	9/2009	• iPod Touch (3rd gen.)
<b>A4</b>	APL0398 or S5L8930		45 nm	53.3 mm <sup>2</sup>	1x Cortex-A8 0.8–1.0 GHz	ARMv7	L1i: 32 KB L1d: 32 KB L2: 512 KB	PowerVR SGX535 @ 200–250 MHz (1.6–2 GFLOPS)	256 MB (iPad) 512 MB (iPhone 4) 32-bit DCh LPDDR-400 (3.2 GB/sec)	3/2010	<ul style="list-style-type: none"> <li>• iPad (1st gen.)</li> <li>• iPhone 4</li> <li>• iPod Touch (4th gen.)</li> <li>• Apple TV (2nd gen.)</li> </ul>



### 3. Apple A4 (3)

#### Main features of the A4 PoP [17]

- The **A4 PoP** incorporates
  - the **A4 SOC** and
  - and **128 MB later 512MB LPDDR 400 SDRAM stacked** memory (via 2x32-bit memory channels).
- The **A4 SOC** includes among others
  - a **single core ARM Cortex A8 CPU** supporting the ARMv7 ISA, it is a **dual-issue in order design**, clocked at 800 MHz and including 512 kB L2,
  - **dual core PowerVR SGX 535 GPU**, clocked at 200 MHz,
- The internal designation of the A4 PoP is S5L8930X.
- The Pop was fabricated by Samsung on a **45 nm** process.
- The die size is 53 mm<sup>2</sup>.

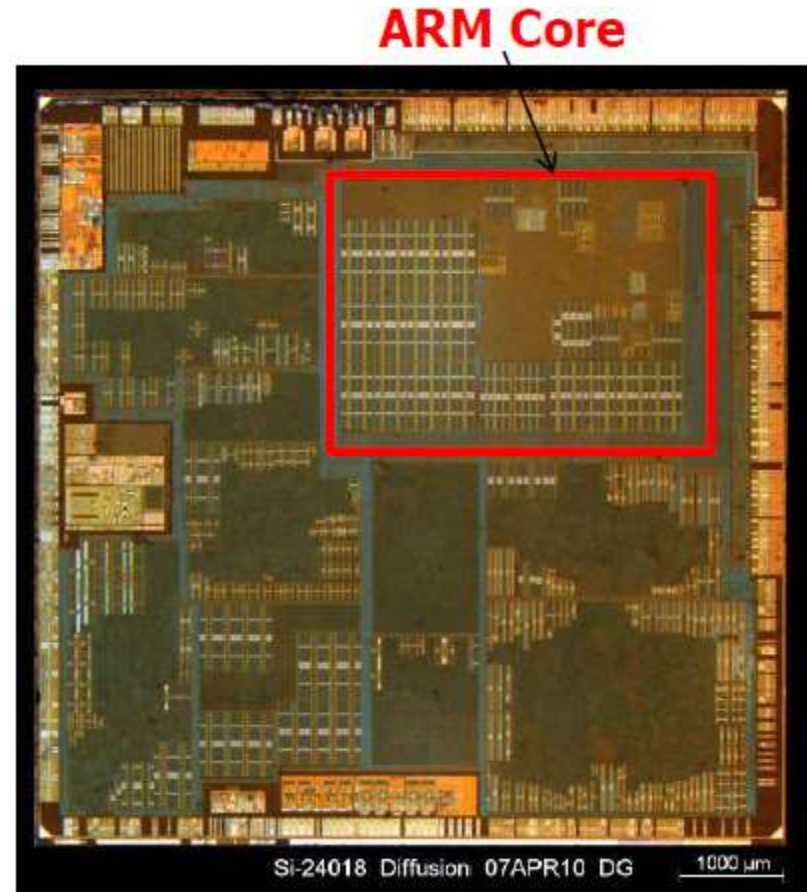
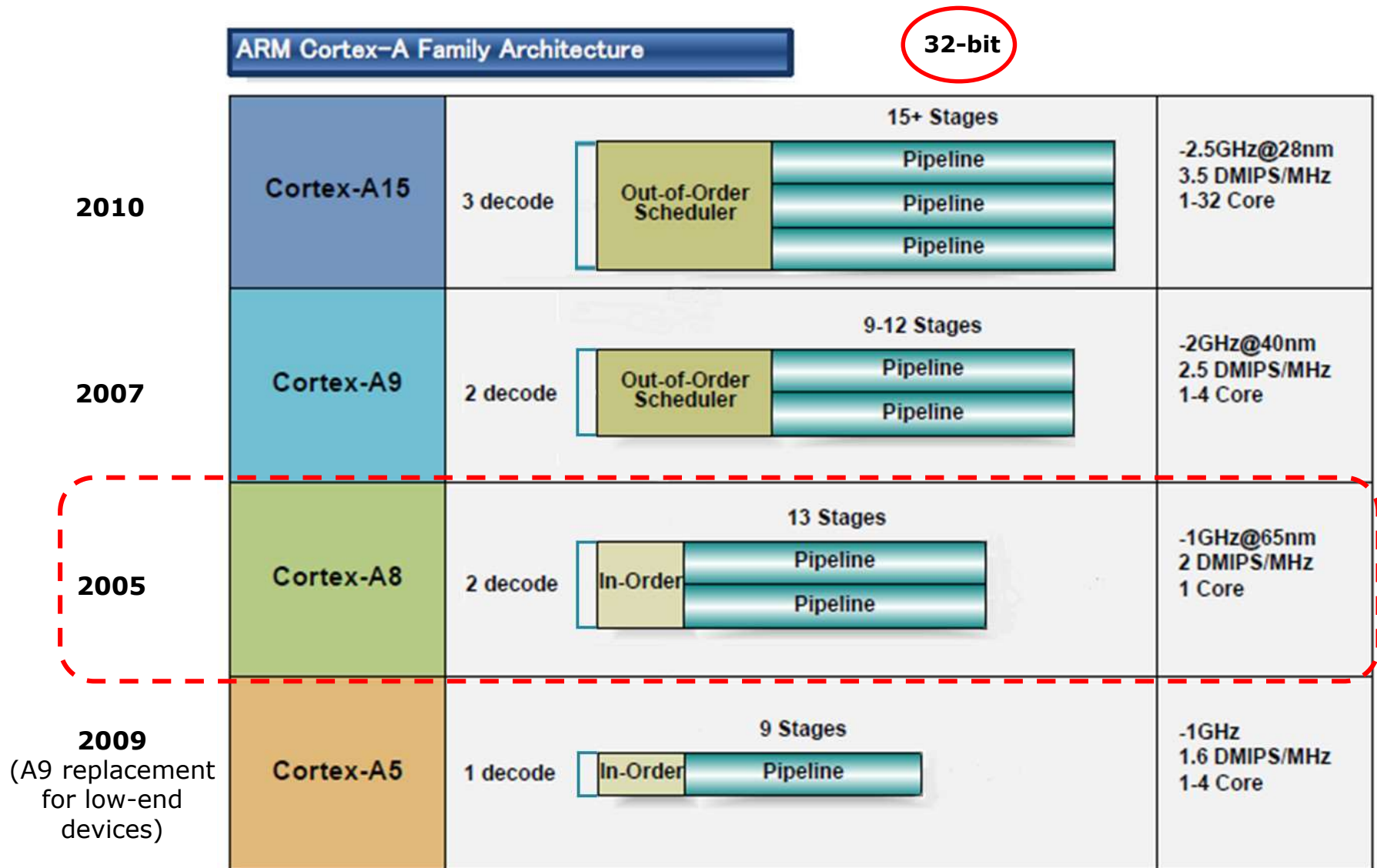


Figure: Die plot of the A4 [17]

### 3. Apple A4 (4)

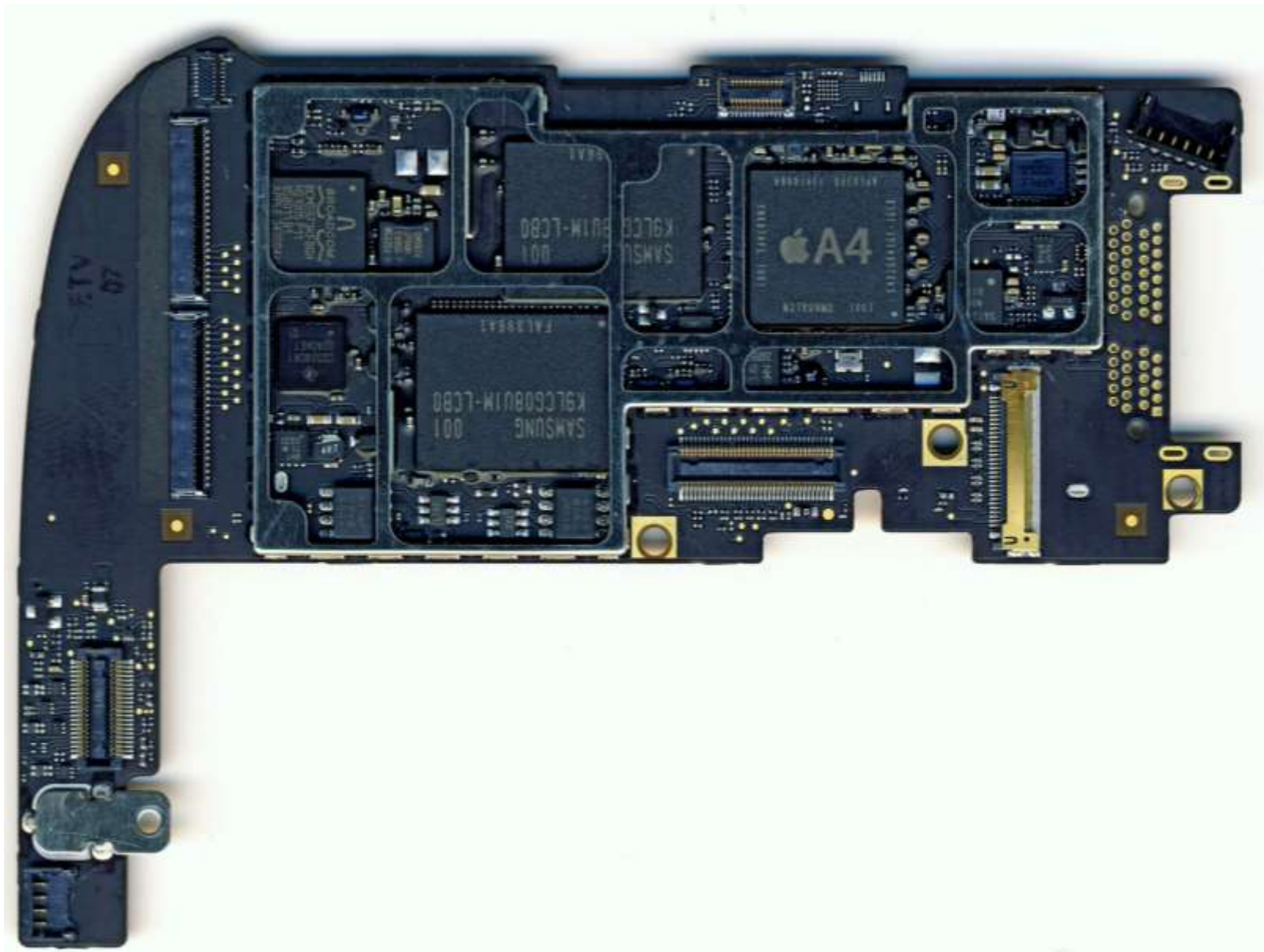
Key features of the microarchitecture of ARM's 32-bit Cortex-A8 core [2]





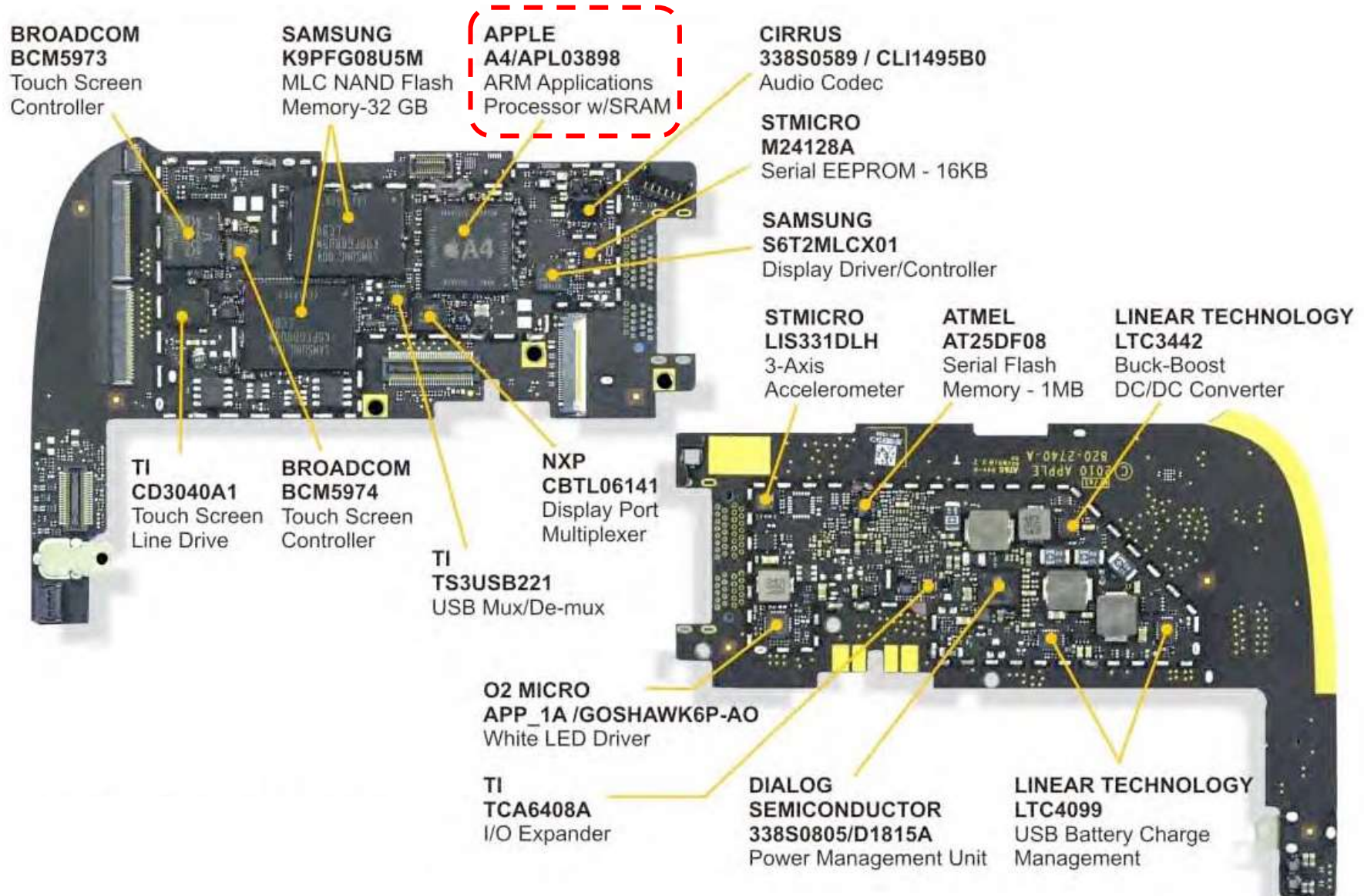
### 3. Apple A4 (5)

The iPad board-1 [12]



### 3. Apple A4 (6)

#### The iPad board-2 [18]



## 4. Apple A6 with dual Swift cores

## 4. Apple A6 with dual Swift cores (1)




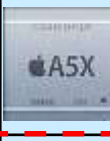


### 4. Apple A6 with dual Swift cores

#### Introduction of the A6

- It debuted in the [iPhone5](#) (2012).
- The **A6** is [Apple's first own in-house design](#), it implements the [ARMv7S ISA](#).  
The S tag indicates an ISA extension implemented for the A6 (Swift) processor.

## 4. Apple A6 with dual Swift cores (2)

### Main features of the A6

Appl. proc.	Model no.	Image	Node	Die size	CPU ISA	CPU	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A5</b>	APL0498 or S5L8940		45 nm	122.2 mm <sup>2</sup>	ARMv7	0.8–1.0 GHz 2C Cortex-A9	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP2 (2C) @ 200–250 MHz (12.8–16 GFLOPS)	512 MB 32-bit DCh LPDDR2-800 (6.4 GB/sec)	3/2011	<ul style="list-style-type: none"> <li>• iPad 2</li> <li>• iPhone 4S</li> </ul>
	APL2498 or S5L8942		32 nm HKMG	69.6 mm <sup>2</sup>	ARMv7	0.8–1.0 GHz 2C Cortex-A9	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP2 (2C) @ 200–250 MHz (12.8–16 GFLOPS)	512 MB 32-bit DCh LPDDR2-800 (6.4 GB/sec)	3/2012	<ul style="list-style-type: none"> <li>• iPad 2 (iPad2,4)</li> <li>• iPod Touch (5th gen.)</li> <li>• iPad Mini</li> </ul>
	APL7498 or S5L8947		32 nm HKMG	37.8 mm <sup>2</sup>	ARMv7	SC Cortex-A9	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP2 (2C) @ 200–250 MHz (12.8–16 GFLOPS)	512 MB 32-bit DCh LPDDR2-800 (6.4 GB/sec)	3/2013	<ul style="list-style-type: none"> <li>• AppleTV 3 (AppleTV3,2)</li> </ul>
<b>A5X</b>	APL5498 or S5L8945		45 nm	165 mm <sup>2</sup>	ARMv7	1.0 GHz 2C Cortex-A9	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP4 (4C) @ 250 MHz (32 GFLOPS)	1 GB 32-bit 4Ch LPDDR2-800 (12.8 GB/sec)	3/2012	<ul style="list-style-type: none"> <li>• iPad (3rd gen.)</li> </ul>
<b>A6</b>	APL0598 or S5L8950		32 nm HKMG	96.71 mm <sup>2</sup>	ARMv7s	1.3 GHz 2C Swift	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX543MP3 (3C) @ 266 MHz (25.5 GFLOPS)	1 GB 32-bit DCh LPDDR2-1066 (8.528 GB/sec)	9/2012	<ul style="list-style-type: none"> <li>• iPhone 5</li> <li>• iPhone 5C</li> </ul>
<b>A6X</b>	APL5598 or S5L8955		32 nm HKMG	123 mm <sup>2</sup>	ARMv7s	1.4 GHz 2C Swift	L1i: 32 KB L1d: 32 KB L2: 1 MB	PowerVR SGX554MP4 (4C) @ 266 MHz (68.1 GFLOPS)	1 GB 32-bit 4Ch LPDDR2-1066 (17.1 GB/sec)	10/2012	<ul style="list-style-type: none"> <li>• iPad (4th gen.)</li> </ul>

## 4. Apple A6 with dual Swift cores (3)

### Remarks to the development of the A6 [19]

- In 4/2008 Apple acquired PA Semi, a CPU design firm that had experience in developing high performance PowerPC processors.  
Previously, some of the team even took part also in the design of the low-power StrongArm processor, at Digital Equipment Corporation.
- About this time Apple also signed a licensing agreement with ARM to be able to implement ARM compatible processors.
- One group of the PA Semi employees set to work on the Apple A4, based on the ARM Cortex A8 core whereas the other group began to define the microarchitecture of the A6 core, designated as Swift.
- In early 2010 the team completed the logical design of the microarchitecture of the A6 core and started with the physical design phase.



## 4. Apple A6 with dual Swift cores (4)

### Main features of the A6 (Swift) PoP [17]

- The **A6 PoP** incorporates
  - the **A6 SOC** and
  - **1GB LPDDR2-1066 SDRAM**  
(via 2x32-bit memory channels).
- the **A6 SOC** includes among others
  - **dual Swift CPU cores**  
supporting the ARMv7s ISA  
(enhanced ARMv7 for Swift),  
it is a **3-wide out-of-order design**,  
clocked at 1.3 GHz and  
including 1 1MB L2,
  - **three core PowerVR SGX 545 GPU**,  
clocked at 333 MHz.
- The internal designation of the A6 PoP is S5L8930X.
- The PoP was fabricated by Samsung on a **32 nm** process.
- The die size is 97 mm<sup>2</sup>.



Figure: The A6 SOC [17]

## 4. Apple A6 with dual Swift cores (5)

Main features of the A6 SOC compared with previous Apple processors [20]

	Apple A4	Apple A5	Apple A5r2	Apple A5X	Apple A6
<b>Intro Date</b>	2010	2011	2012	2012	2012
<b>Intro Product</b>	iPad	iPad 2	iPad 2	iPad 3	iPhone 5
<b>Product Targets</b>	iPad/iPhone 4	iPad 2/iPhone 4S	iPad 2/iPhone 4S	iPad 3	?
<b>CPU</b>	ARM Cortex A8	2 x ARM Cortex A9	2 x ARM Cortex A9	2 x ARM Cortex A9	2 x Apple Swift
<b>CPU Frequency</b>	1GHz/800MHz (iPad/iPhone)	1GHz/800MHz (iPad/iPhone)	1GHz/800MHz (iPad/iPhone)	1GHz	1.3GHz
<b>GPU</b>	PowerVR SGX 535	PowerVR SGX 543MP2	PowerVR SGX 543MP2	PowerVR SGX 543MP4	PowerVR SGX 543MP3
<b>Memory Interface</b>	32-bit LPDDR2	2 x 32-bit LPDDR2	2 x 32-bit LPDDR2	4 x 32-bit LPDDR2	2 x 32-bit LPDDR2
<b>Manufacturing Process</b>	Samsung 45nm LP	Samsung 45nm LP	Samsung 32nm LP HK+MG	Samsung 45nm LP	Samsung 32nm LP HK+MG



## 4. Apple A6 with dual Swift cores (6)

### Microarchitecture of the Swift core

- The A6 is Apple's (first and single) **3-issue out-of-order superscalar** with a **dispatch rate of 4**, as indicated in the next Figure.

## 4. Apple A6 with dual Swift cores (7)

### Width of mobile cores

#### Width of mobile cores (or of big cores of big.LITTLE or dynamIQ core clusters)

2-wide

3-wide

4-wide

6-wide

ARM

v7 ISA based  
(32-bit) Cortex-A cores  
except the Cortex-A15)  
(2005-2009)



v7 ISA based  
(32-bit) Cortex-A15  
(2010)

v8 ISA-based  
Cortex-A73 (2016)



v8 ISA-based  
(64-bit) Cortex-A line,  
except the Cortex-A73 (2012-)

Intel

Atom family  
(2008-2016)

AMD

Cat family  
(2011-2015)

Apple

Cortex-A8 (2009)



A6 (Swift (2012))



A7 (Cyclone (2013))  
and subsequent cores

Qualcomm

Scorpion v7 ISA  
(S1-S3) (2007-2010)



Krait v7 ISA  
(S4/S400/S60x/S80x)  
(2012-2014)

Kryo/Kryo 280 v8 ISA  
(S820/821/835)  
(2015/2016/2017)

Kryo 385 v8.2 ISA  
(S845) (2018)

Samsung

Exynos 5 v7 ISA  
(2013-2014)



/Exynos 7 v8 ISA  
(2016)

M1 core v8 ISA (2016)  
(Exynos 8 Octa)

M2 core v8 ISA (2017)  
(Exynos 9 Octa)

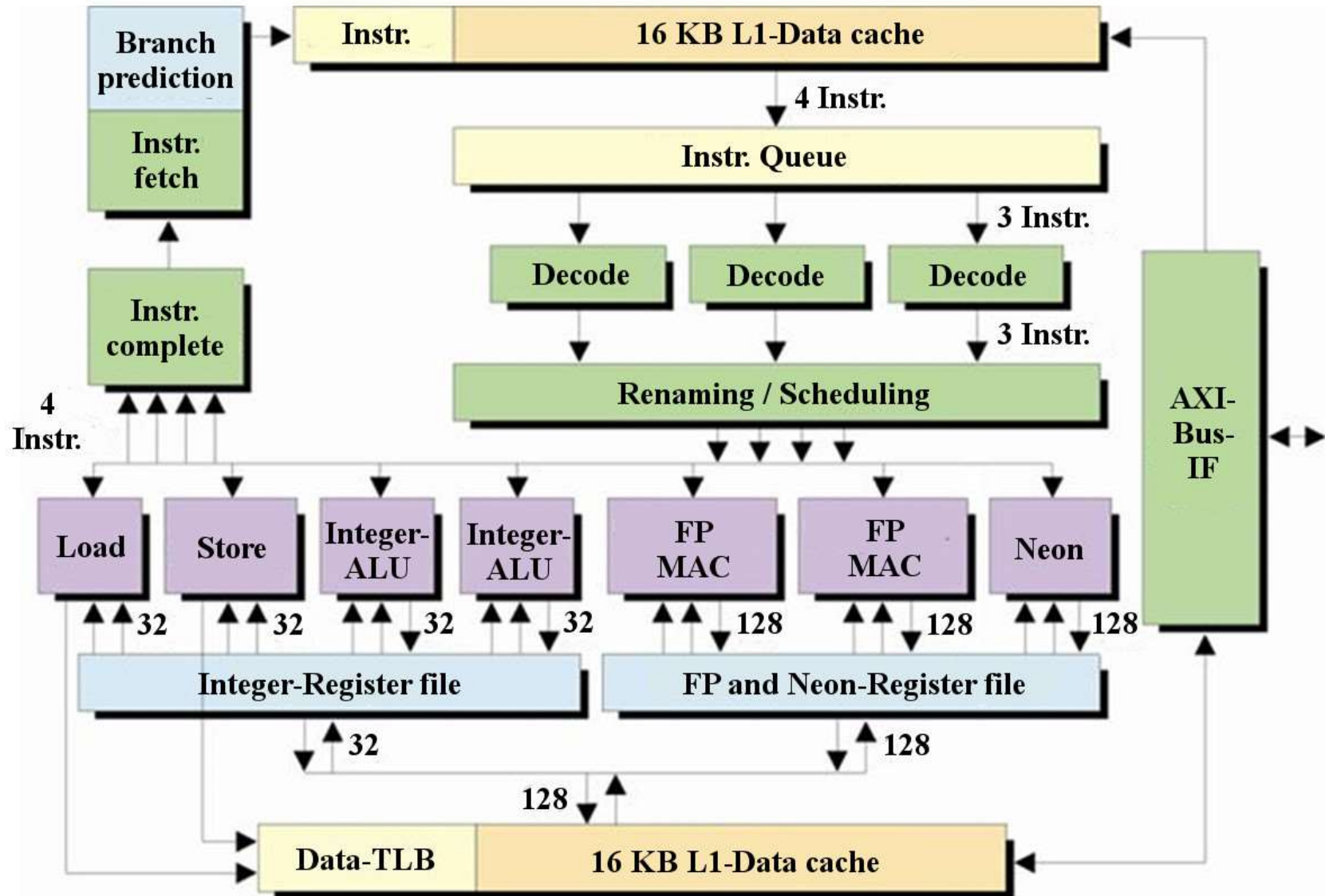


M3 core v8.2 ISA  
(2018)

(Exynos 9810)

## 4. Apple A6 with dual Swift cores (8)

Assumed block diagram of the Swift core [21]









## 5. Apple A7 with dual Cyclone cores

### 5. Apple A7 with dual Cyclone cores

- The **A7** emerged in the mobile devices
  - iPhone 5S
  - iPad Mini 2
  - iPad Mini 3 and
  - iPad Airin 2013.
- It is **Apple's second own in-house design**, it implements the **ARMv8-A ISA**, that is the **64-bit ARMv8 ISA with custom Apple extensions**.

## 5. Apple A7 with dual Cyclone cores (2)

### Main features of the A7 -1

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A7</b>	APL0698 or S5L8960		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.3 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2013	iPhone 5S iPad Mini 2 iPad Mini 3
	APL5698 or S5L8965		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	10/2013	iPad Air 9.7"
<b>A8</b>	APL1011		20 nm HKMG	89 mm <sup>2</sup>	2x Typhoon 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR GX6450 (4C) @ 450 MHz (115.2 GFLOPS)	1GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2014	iPhone 6 iPhone 6 Plus
<b>A8X</b>	APL1012		20 nm HKMG	128 mm <sup>2</sup>	3xTyphoon 1.5 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 2 MB L3: 4 MB	PowerVR GX6850 (5C) @ 450 MHz (230.4 GFLOPS)	2 GB 64-bit DCh LPDDR3-1600 (25.6 GB/sec)	10/2014	iPad Air 2 9.7"
<b>A9</b>	APL1022 (TSMC) APL0898 (Samsung)		16 nm FinFET 14 nm FinFET	104.5 mm <sup>2</sup>	2xTwister 1.85 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: 4 MB	PowerVR GT7600 (6C) @ 450 MHz (172.8 GFLOPS)	2 GB 64-bit SCh LPDDR4-3200 (25.6 GB/sec)	9/2015	iPhone 6s iPhone 6s Plus iPhone SE
<b>A9X</b>	APL1021 (TSMC)		16 nm FinFET	147 mm <sup>2</sup>	2xTwister 2.16-2.26 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: none	PowerVR 7XT series (12C) @ n.a. MHz (345.6 GFLOPS)	2 GB/4 GB 64-bit DCh LPDDR4-3200 (51.2 GB/sec)	11/2015 (12.9") 3/2016 (9.7")	iPad Pro 9.7" iPad Pro 12.9"

## 5. Apple A7 with dual Cyclone cores (3)

### Main features of the A7 -2 [10]

- It has **dual CPU cores**, called **Cyclone** cores.
- The out-of-order cores are **6-wide**.
- The clock rate is 1.3 GHz.
- The cores have a shared 1 MB L2 and a shared 4 MB L3 (first in the A line).
- The GPU is a PowerVR 6430 with four cores, clocked at 1.3 GHz.
- The **A7 PoP** includes also a 1 GB **stacked SDRAM** (LPDDR3-1600 SDRAM (attached via 2x32-bit memory channels)).

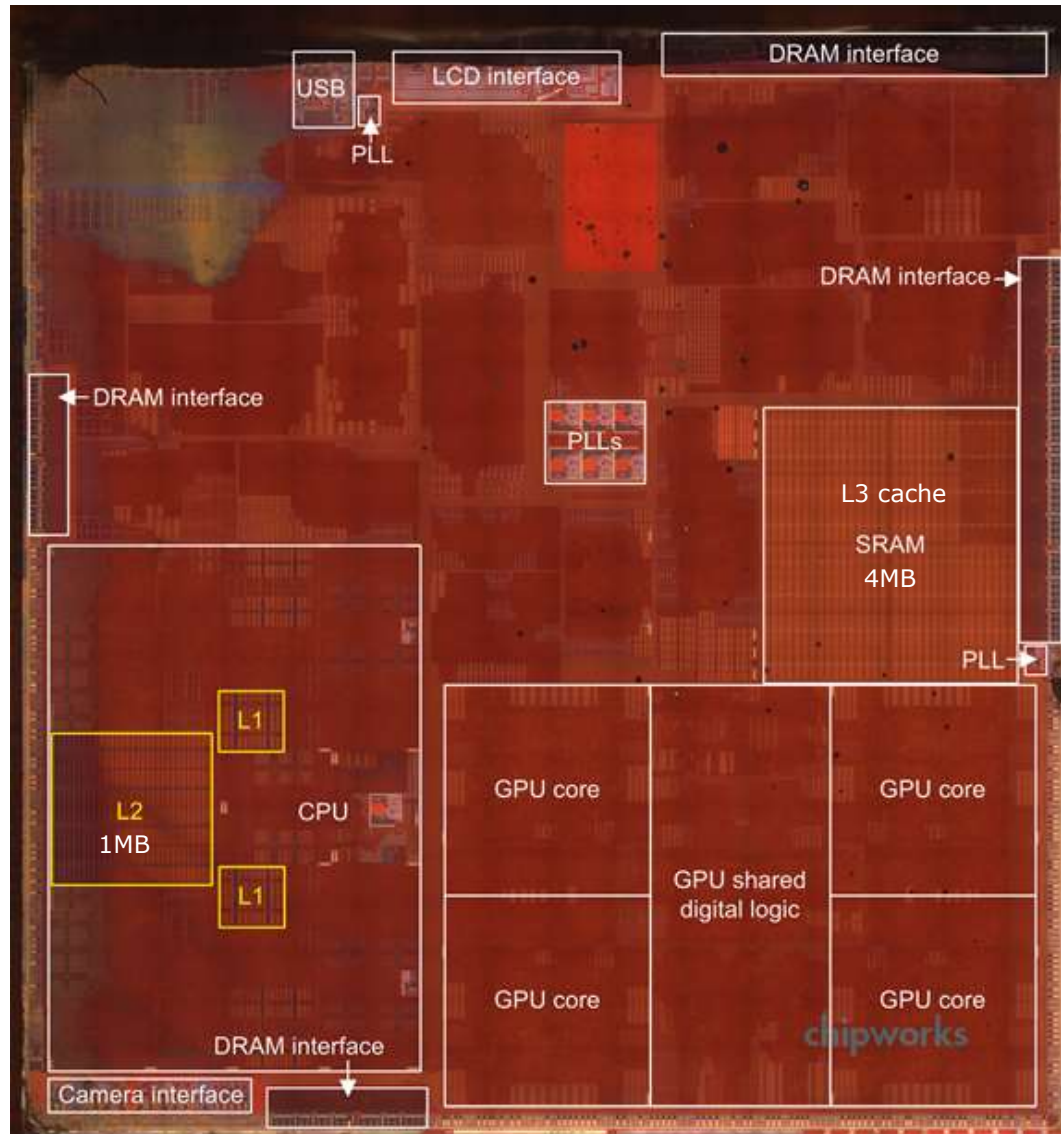


Figure: The A7 SOC [10]



## 5. Apple A7 with dual Cyclone cores (4)

### Main features of the A7 -3 [10]

- The internal designation of the A7 PoP is S5L8960X.
- The PoP was fabricated by Samsung on a **28 nm** process.
- The die size is 102 mm<sup>2</sup>.
- The **transistor count** is **~ 1 billion**.

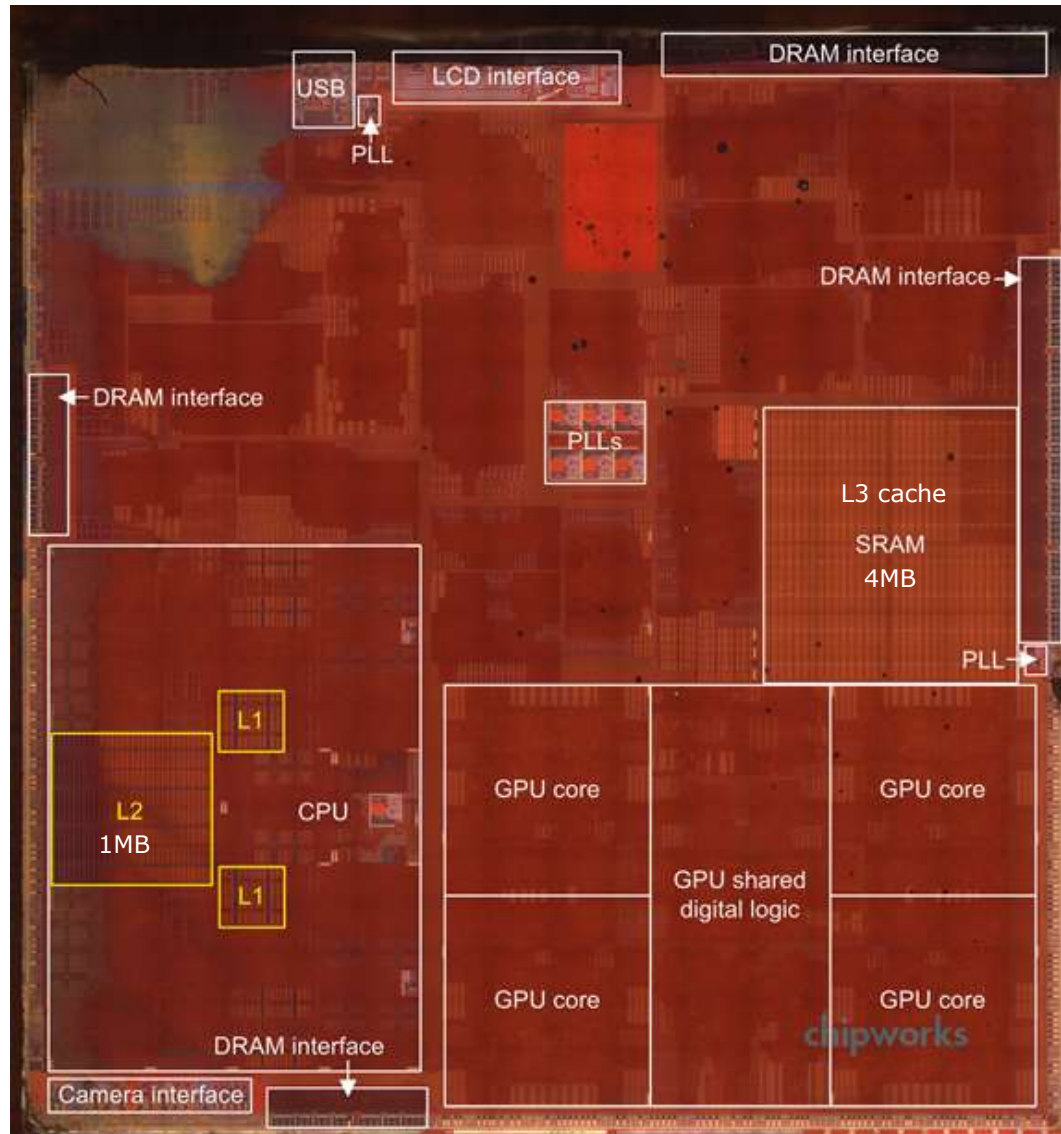


Figure: The A7 SOC [10]



## 5. Apple A7 with dual Cyclone cores (5)

Using a motion coprocessor (designated as M7) to reduce the load on the A7 [22], [23]

- The iPhone 5S, iPad mini 2, 3 or the iPad Air A7 also include a **motion coprocessor**, designated as **M7**.
- It is actually an **ARM Cortex-M3** microcontroller running at 180 MHz.
- The chip **collects information from sensors**, such as the accelerometer, gyroscope or magnetometer, **processes these data and forwards workable data to the A7**. Health and fitness **apps can then make use of these data** e.g. for distinguishing the type or speed of the motion currently taking place etc..
- The low power M7 **reduces the load on the A7** chip and greatly improves in this way battery life.
- Subsequent implementations of Apple's mobile devices continue to make use of motion coprocessors (designated as the M8 for the A8 and A8X SOCs).

## 5. Apple A7 with dual Cyclone cores (6)

### Microarchitecture of the Cyclone core-1

- Apple does not reveal any details of their processor microarchitectures.
- Nevertheless, in order to support LLVM compiler optimization [Apple revealed the machine model of the Cyclone core](#) as follows.

## 5. Apple A7 with dual Cyclone cores (7)

Part of the machine model of the Cyclone core as revealed by Apple [24]

```
//====-----//
//
// This file defines the machine model for ARM64 Cyclone to support
// instruction scheduling and other instruction cost heuristics.
//
//====-----//

def CycloneModel : SchedMachineModel {
  let IssueWidth = 6; // 6 micro-ops are dispatched per cycle.
  let MicroOpBufferSize = 192; // Based on the reorder buffer.
  let LoadLatency = 4; // Optimistic load latency.
  let MispredictPenalty = 16; // 14-19 cycles are typical.
}

//====-----//
// Define each kind of processor resource and number available on Cyclone.

// 4 integer pipes
def CyUnitI : ProcResource<4> {
  let BufferSize = 48;
}

// 2 branch units: I[0..1]
def CyUnitB : ProcResource<2> {
  let Super = CyUnitI;
  let BufferSize = 24;
}
```

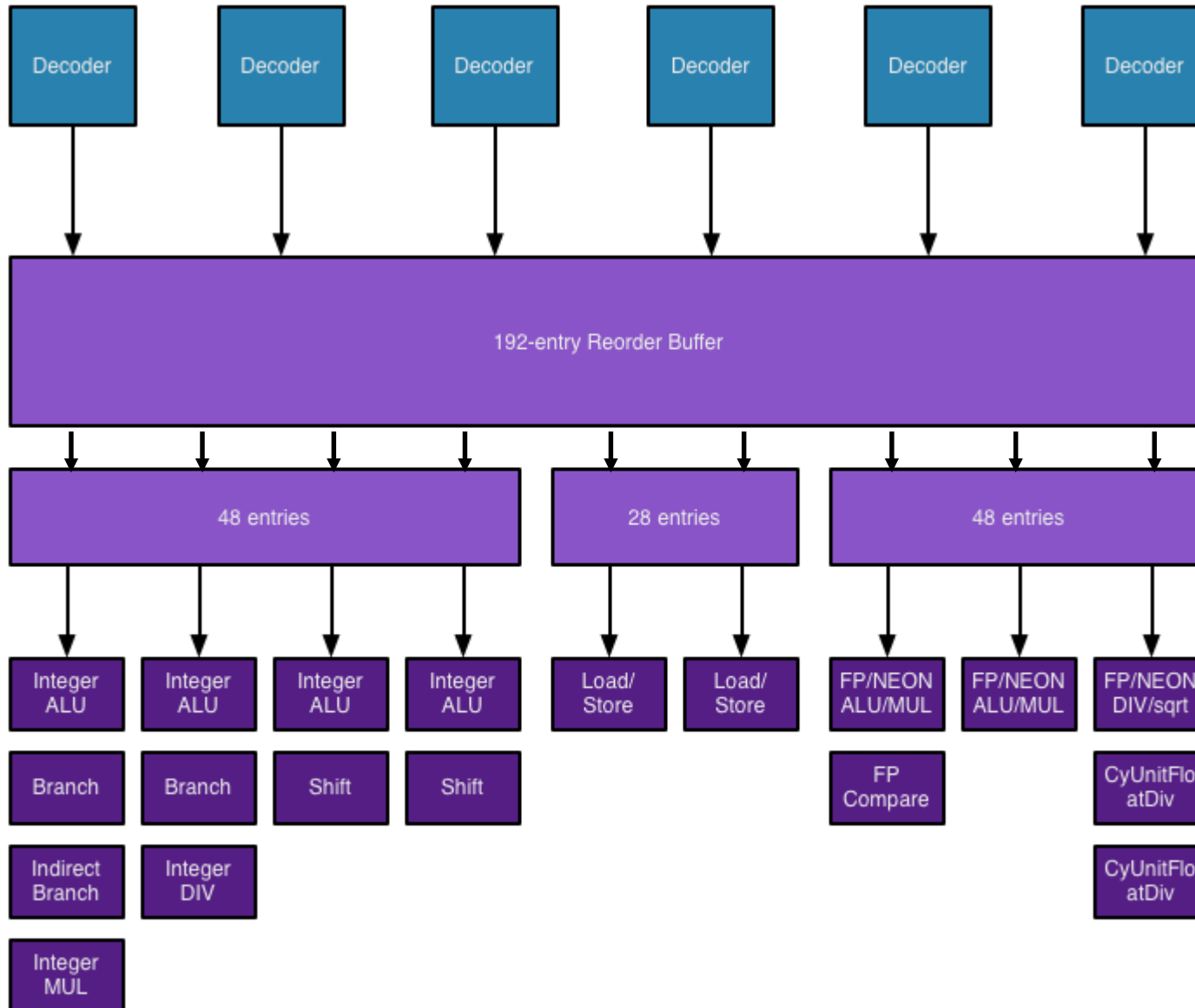
## 5. Apple A7 with dual Cyclone cores (8)

### Microarchitecture of the Cyclone core-2

Based on the above compiler specifications, Cyclone's microarchitecture was guessed in two publications, as shown next.

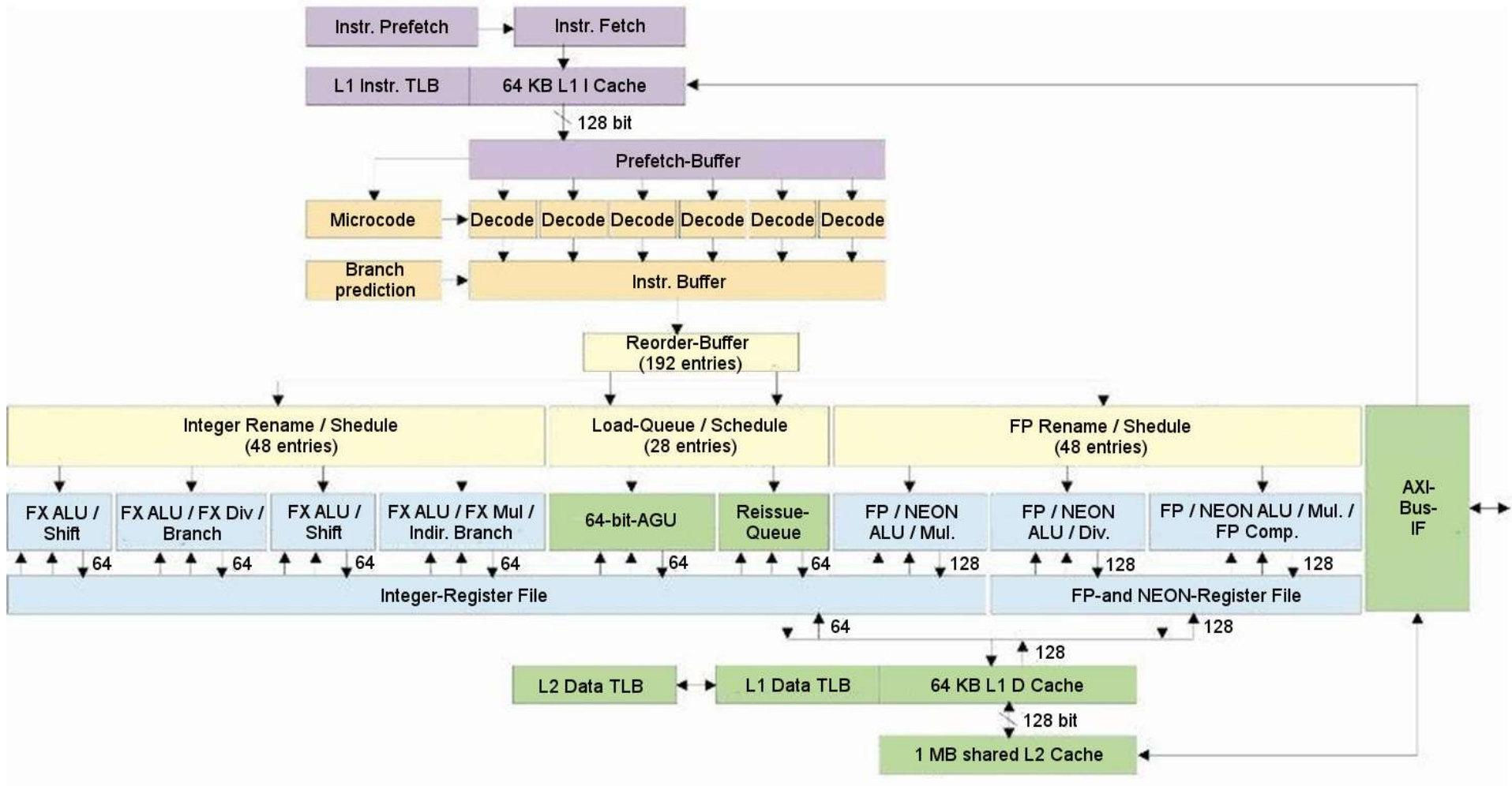
## 5. Apple A7 with dual Cyclone cores (9)

Assumed block diagram of the Cyclone core, based on [25]



## 5. Apple A7 with dual Cyclone cores (10)

Assumed block diagram of the Cyclone core, based on [26]



## 5. Apple A7 with dual Cyclone cores (11)

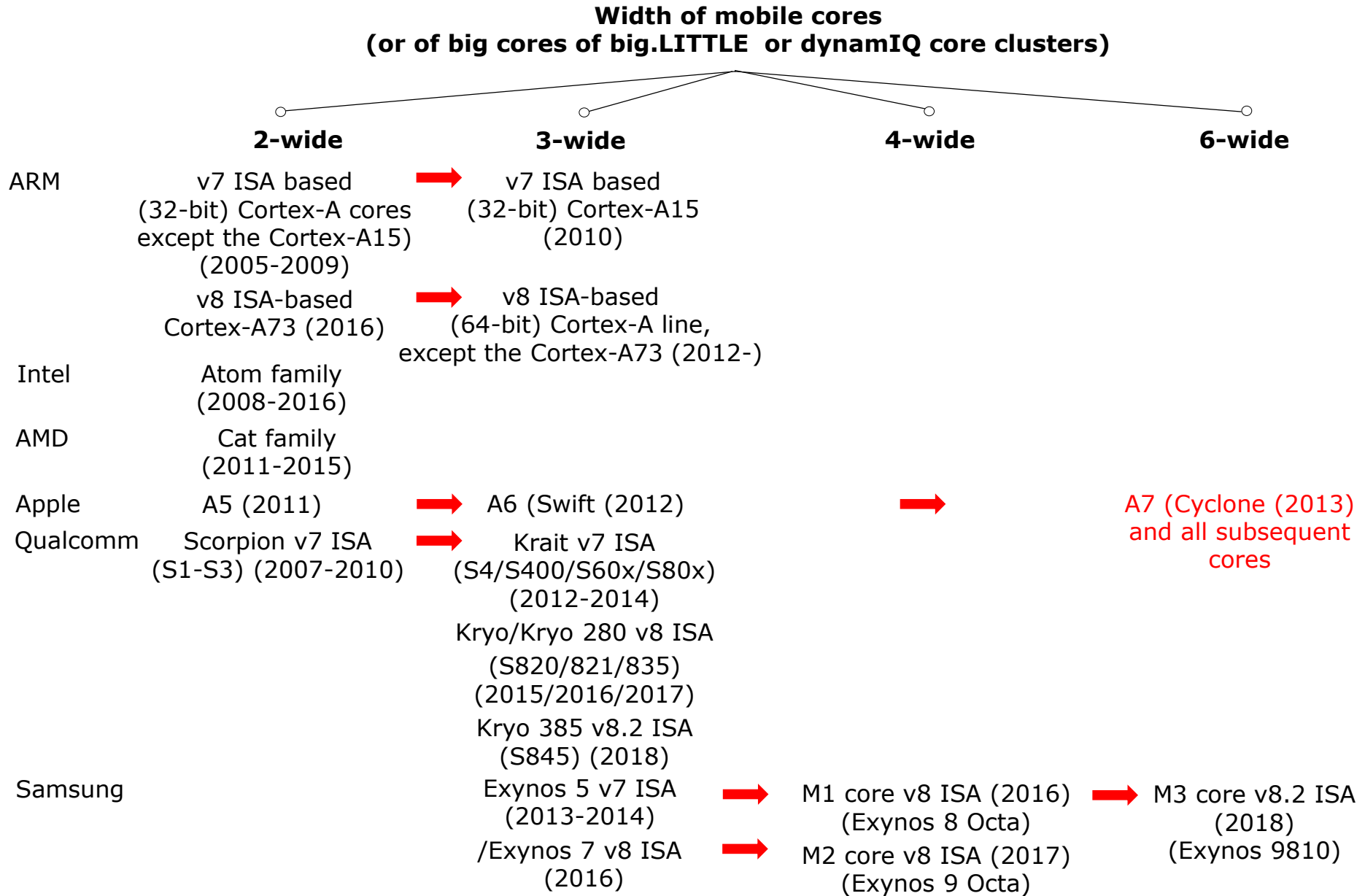
### Microarchitecture of the Cyclone core-3

- As seen, the Cyclone core is an extremely wide - 6-wide - out-of-order superscalar with an issue rate of 9.
- In contrast, even Intel's and AMD's recent performance/Watt oriented processors such as Haswell, Broadwell, Bulldozer or Piledriver are only 4-wide designs, as indicated in the next Figures.



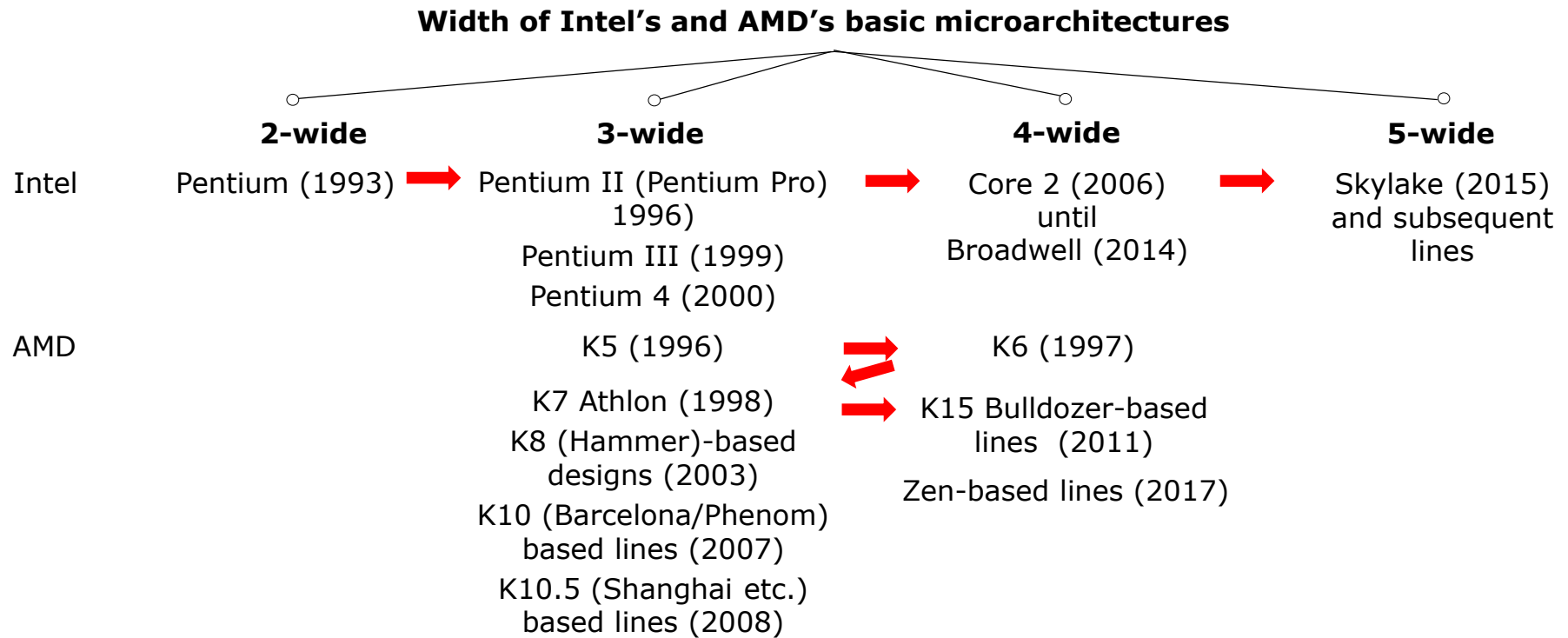
# 5. Apple A7 with dual Cyclone cores (12)

## Width of mobile cores



## 5. Apple A7 with dual Cyclone cores (13)

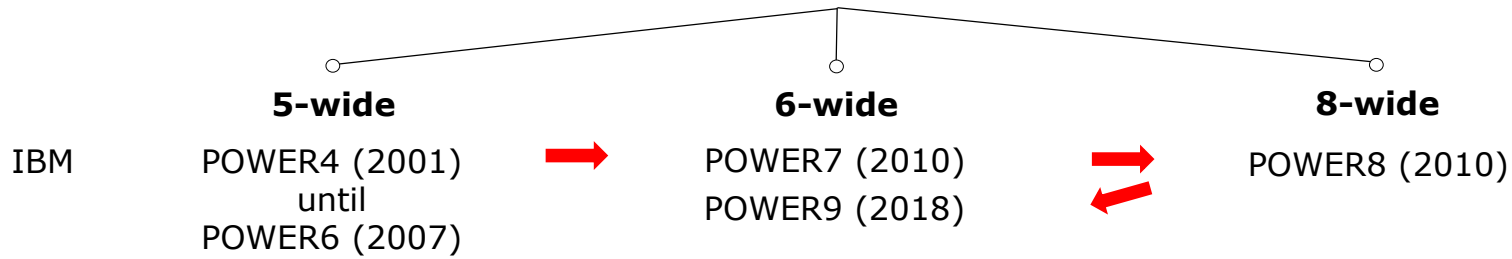
### Width of Intel's and AMD's basic microarchitectures



## 5. Apple A7 with dual Cyclone cores (14)

### Width of IBM's POWER microarchitectures

#### Width of IBM's POWER microarchitectures



## 5. Apple A7 with dual Cyclone cores (15)

Contrasting key features of the A6 and A7 microarchitectures [25]

	Apple A6	Apple A7
CPU Codename	Swift	Cyclone
ARM ISA	ARMv7-A (32-bit)	ARMv8-A (32/64-bit)
Issue Width	3 micro-ops	6 micro-ops
Reorder Buffer Size	45 micro-ops	192 micro-ops
Branch Mispredict Penalty	14 cycles	16 cycles (14 - 19)
Integer ALUs	2	4
Load/Store Units	1	2
Load Latency	3 cycles	4 cycles
Branch Units	1	2
Indirect Branch Units	0	1
FP/NEON ALUs	?	3
L1 Cache	32KB I\$ + 32KB D\$	64KB I\$ + 64KB D\$
L2 Cache	1MB	1MB
L3 Cache	-	4MB

## 5. Apple A7 with dual Cyclone cores (16)

Performance comparison of Apple processors [27]

Geekbench 3 Scores		
	Single-Thread	Multi-Thread
iPad Air 2    A8X   3C	1798	4468
iPhone 6     A8     2C	1610	2881
iPad Air      A7     2C	1472	2663
iPad 4        A6X   2C	770	1401

The benchmark scores for Geekbench 3 show that the 6-wide A7 has approximately twice the performance of the 3-wide A6X.

## 5. Apple A7 with dual Cyclone cores (17)

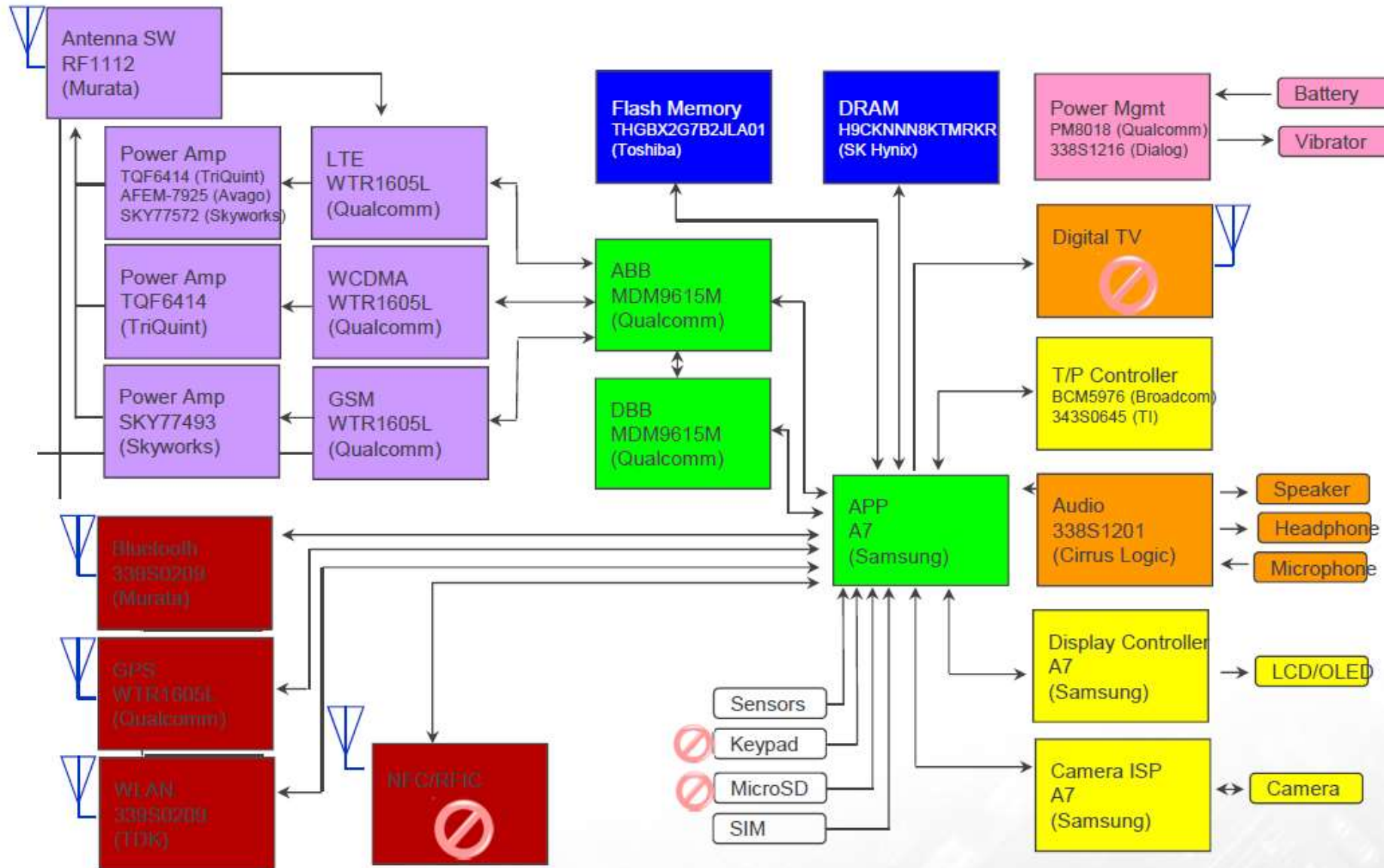
Example: Apple's iPhone 5s xxx and its constituents [10]

Apple iPhone 5s



## 5. Apple A7 with dual Cyclone cores (18)

Assumed block diagram of the Apple iPhone 5s [10]





## 5. Apple A7 with dual Cyclone cores (19)

Display side of the PCB#1 in Apple's iPhone 5s [10]

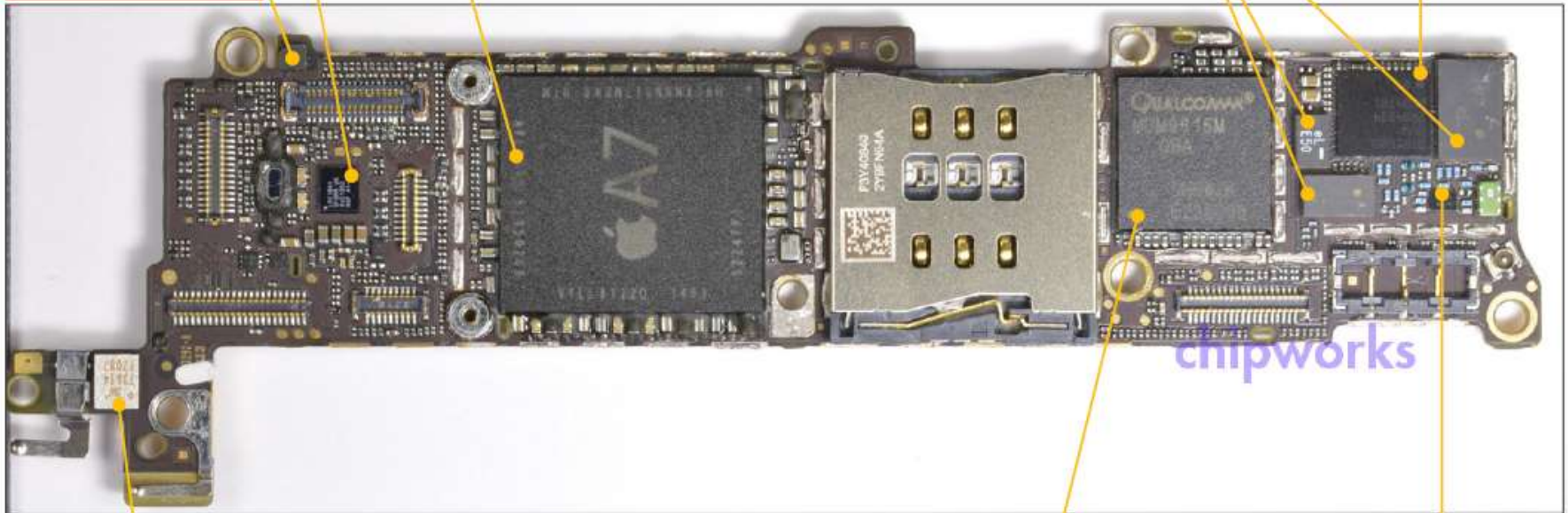
A7 Application Processor (Samsung)  
+ 8 Gb LPDDR3 SDRAM (SK Hynix)  
H9CKNNN8KTMRKR

M7 Co-Processor (NXP)  
LPC18A1

Digital Compass  
(Asahi Kasei)  
AKM8963

LTE/WCDMA/CDMA/GSM Transceiver  
+ GPS (Qualcomm) WTR1605L

Duplexer Banks (Murata)



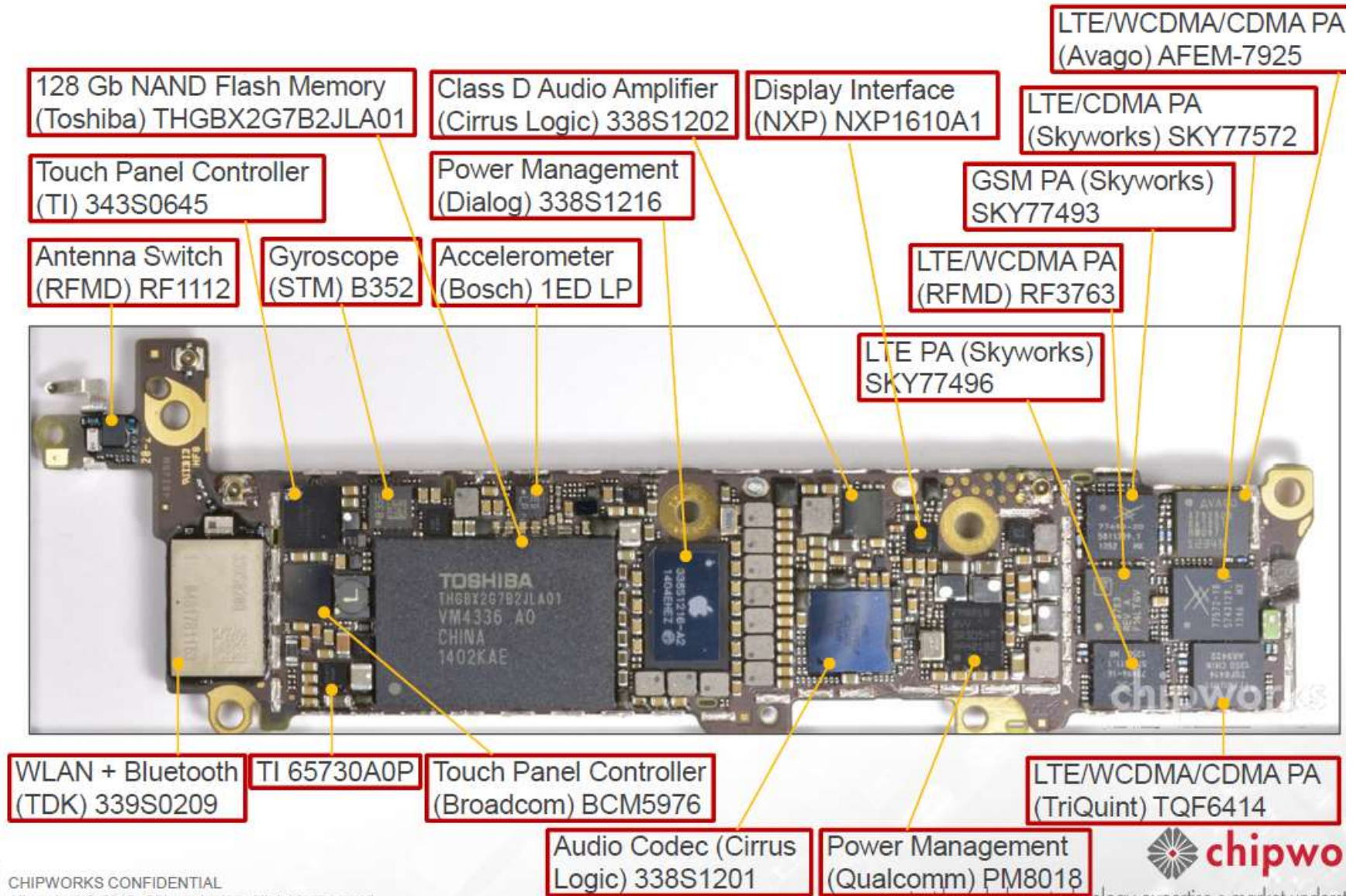
Diversity Down-conversion Mixer  
(Skyworks) SKY73614

Baseband Processor (Qualcomm)  
MDM9615M

Filter (Murata)

## 5. Apple A7 with dual Cyclone cores (20)

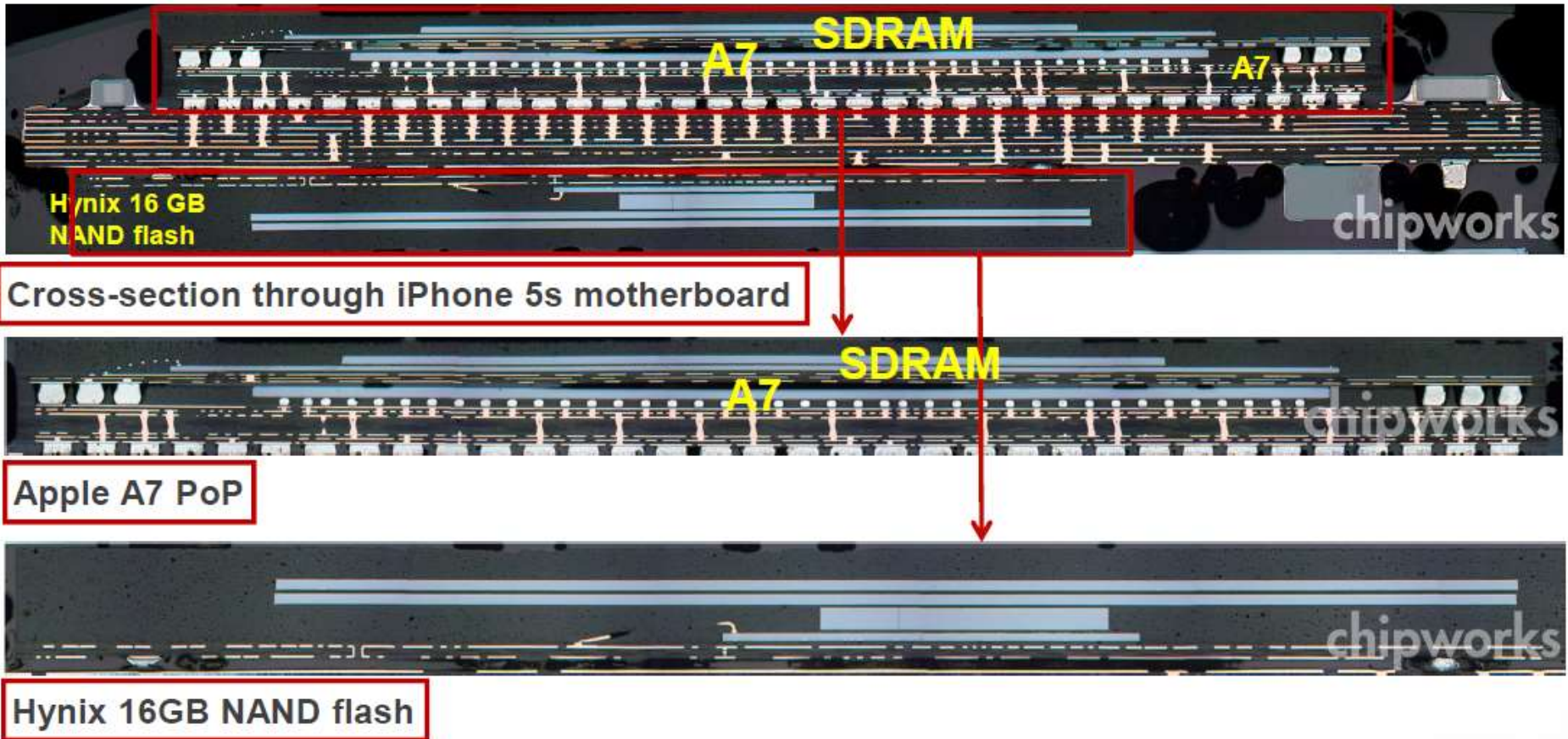
Battery side of the PCB#2 in Apple's iPhone 5s [10]





## 5. Apple A7 with dual Cyclone cores (21)

Apple's A7 Package-on-Package in the iPhone 5s [10]



### Introduction of Apple's own low-level graphics and compute API termed Metal

- According to Apple, the existing **OpenGL ES** framework has interposed **too much overhead between the GPU and the software running on it**, leading to inefficiencies and performance loss.
- In order resolve this problem Apple designed their **own C++-based low-level graphics framework** called **Metal** that was introduced in connection with **iOS 8** in **6/2014**.

## 5. Apple A7 with dual Cyclone cores (23)

### Apple's Metal graphics and compute API -1

- It can be used for [writing GPU code](#) for graphics and general-purpose data-parallel computations in order [to reduce the programming overhead](#) vs. Open GL or Open GL ES (Open GL for Embedded Systems like mobiles).

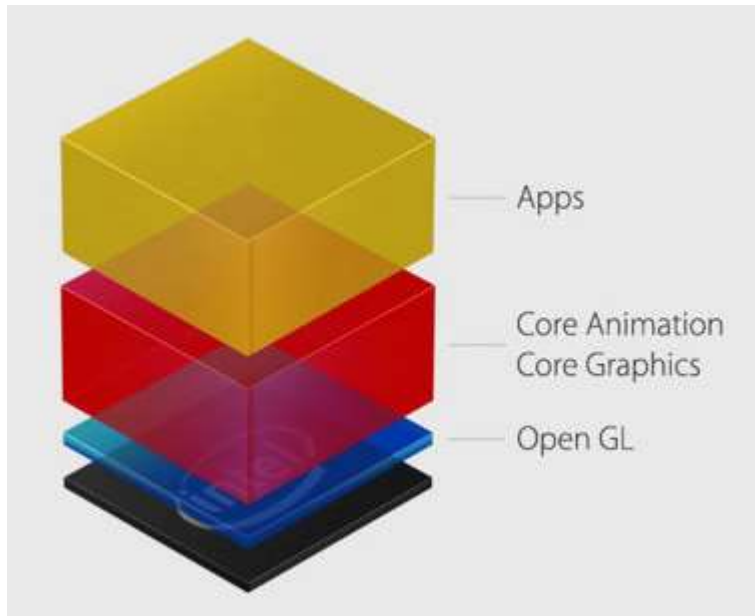


Figure: Using the Open GL graphics API

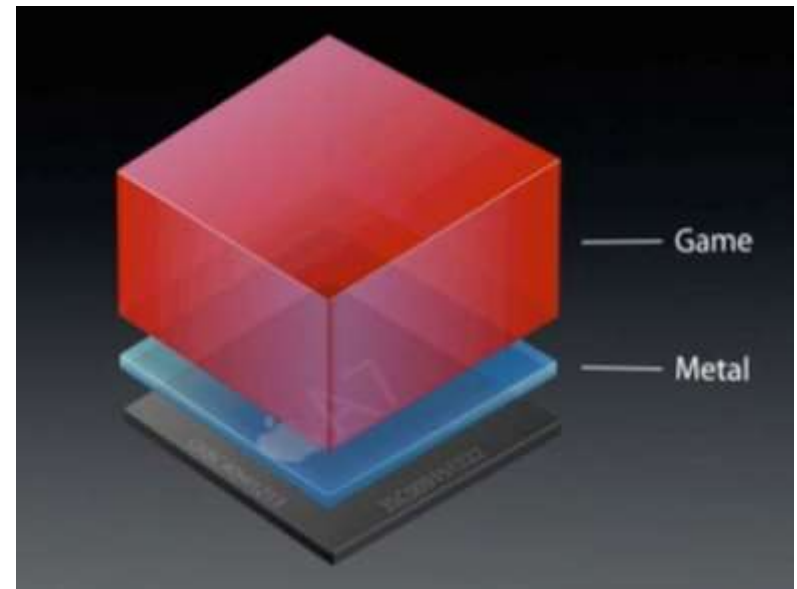
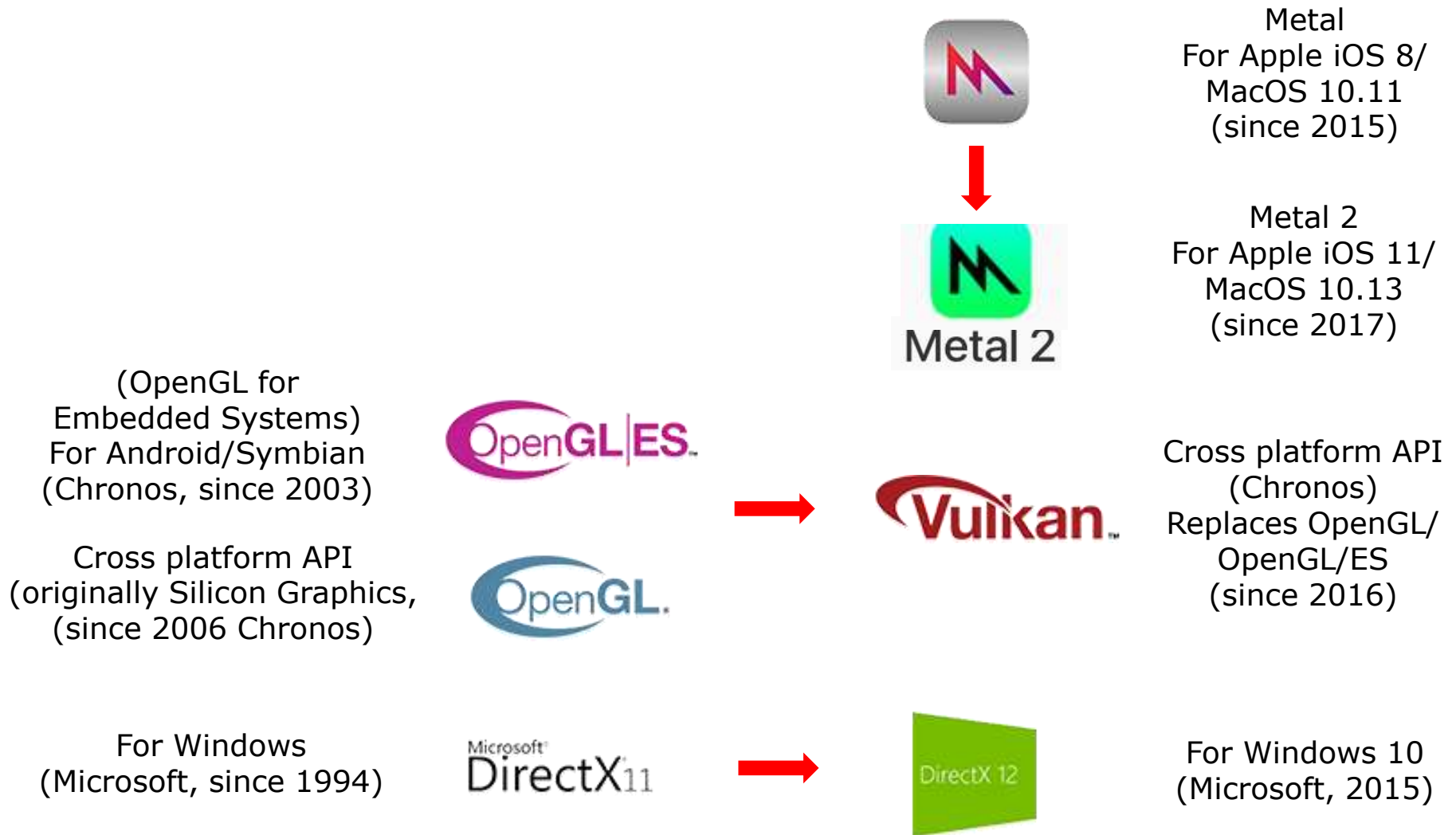


Figure: Using the Metal graphics API

## 5. Apple A7 with dual Cyclone cores (24)

### Low-level graphics and compute APIs



## 6. Apple A8 with dual Typhoon cores



### 6. The Apple A8 with dual Typhoon cores [28]

- The **A8** emerged in the mobile devices
  - iPhone 6 and
  - iPhone 6 Plus






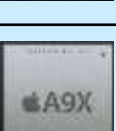
in 2014.

Its microarchitecture is 6-wide, like that of the A7.

- It is a 20 nm shrink of the A7 (fabricated by TSMC rather than Samsung, as previously) with an improved GPU.
- It contains 2 billion transistors, roughly twice than the A7.
- The die size has been reduced by about 13 % to 89 mm<sup>2</sup>.
- The A8 has approximately the same clock speed as the A7 (1.38 GHz).
- The Typhoon core is about 10 % faster than its predecessor (the A7), as indicated in the subsequent Figure for the Geekbench 3 benchmark.

## 6. Apple A8 with dual Typhoon cores (2)

### Main features of the A8

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A7</b>	APL0698 or S5L8960		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.3 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2013	iPhone 5S iPad Mini 2 iPad Mini 3
	APL5698 or S5L8965		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	10/2013	iPad Air 9.7"
<b>A8</b>	APL1011		20 nm HKMG	89 mm <sup>2</sup>	2x Typhoon 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR GX6450 (4C) @ 450 MHz (115.2 GFLOPS)	1GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2014	iPhone 6 iPhone 6 Plus
<b>A8X</b>	APL1012		20 nm HKMG	128 mm <sup>2</sup>	3xTyphoon 1.5 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 2 MB L3: 4 MB	PowerVR GX6450 (5C) @ 450 MHz (230.4 GFLOPS)	2 GB 64-bit DCh LPDDR3-1600 (25.6 GB/sec)	10/2014	iPad Air 2 9.7"
<b>A9</b>	APL1022 (TSMC) APL0898 (Samsung)		16 nm FinFET 14 nm FinFET	104.5 mm <sup>2</sup>	2xTwister 1.85 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: 4 MB	PowerVR GT7600 (6C) @ 450 MHz (172.8 GFLOPS)	2 GB 64-bit SCh LPDDR4-3200 (25.6 GB/sec)	9/2015	iPhone 6s iPhone 6s Plus iPhone SE
<b>A9X</b>	APL1021 (TSMC)		16 nm FinFET	147 mm <sup>2</sup>	2xTwister 2.16-2.26 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: none	PowerVR 7XT series (12C) @ n.a. MHz (345.6 GFLOPS)	2 GB/4 GB 64-bit DCh LPDDR4-3200 (51.2 GB/sec)	11/2015 (12.9") 3/2016 (9.7")	iPad Pro 9.7" iPad Pro 12.9"

## 6. Apple A8 with dual Typhoon cores (3)

Contrasting key features of the A8 vs. the A7 [39]

	Apple A8 (2014)	Apple A7 (2013)
<b>Manufacturing Process</b>	TSMC 20nm HKMG	Samsung 28nm HKMG
<b>Die Size</b>	89mm <sup>2</sup>	102mm <sup>2</sup>
<b>Transistor Count</b>	~2B	"Over 1B"
<b>CPU</b>	2 x Apple Enhanced Cyclone ARMv8 64-bit cores	2 x Apple Cyclone ARMv8 64-bit cores
<b>GPU</b>	IMG PowerVR GX6450	IMG PowerVR G6430

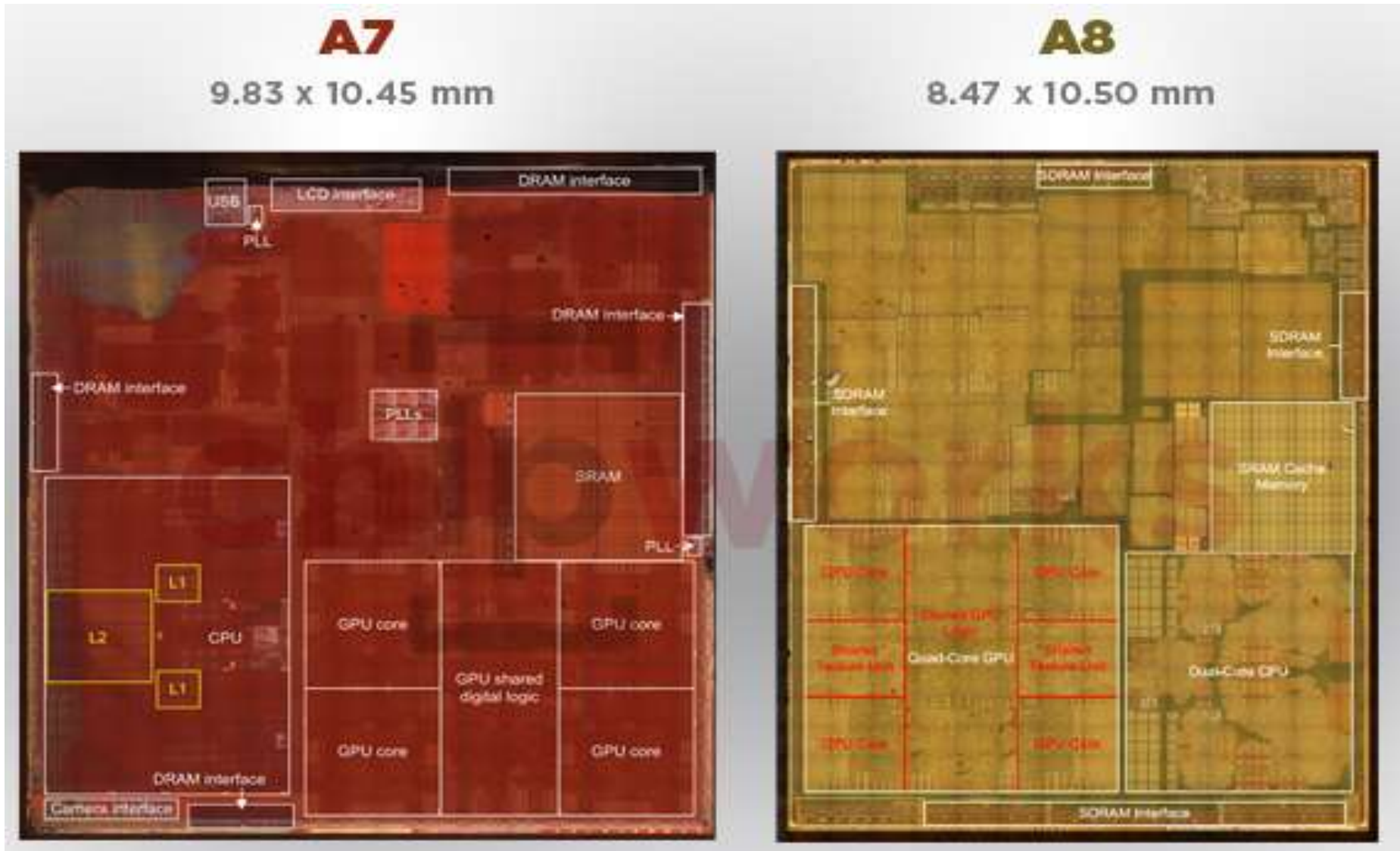
## 6. Apple A8 with dual Typhoon cores (4)

Performance comparison of Apple processors from the A6X to A8X [27]

Geekbench 3 Scores				
			Single-Thread	Multi-Thread
iPad Air 2	A8X	3C	1798	4468
iPhone 6	A8	2C	1610	2881
iPad Air	A7	2C	1472	2663
iPad 4	A6X	2C	770	1401

The benchmark scores for Geekbench 3 show that the A8, i.e. the 20 nm shrink of the 28 nm A7, has approximately 10% performance improvement over the A7.

## Comparing the die plots of A8 and A7 [29]



## 6. Apple A8 with dual Typhoon cores (6)

The assumed microarchitecture of the Typhoon core of the A8 [29]

A8's Typhoon core has basically the same microarchitecture as A7's Cyclone core, as indicated by a comparison vs. the A7 (see next Table).

## 6. Apple A8 with dual Typhoon cores (7)

Contrasting key features of the microarchitectures of the A8 and A7 [39]

	Apple A7	Apple A8
<b>CPU Codename</b>	Cyclone	Typhoon
<b>ARM ISA</b>	ARMv8-A (32/64-bit)	ARMv8-A (32/64-bit)
<b>Issue Width</b>	6 micro-ops	6 micro-ops
<b>Reorder Buffer Size</b>	192 micro-ops	192 micro-ops?
<b>Branch Mispredict Penalty</b>	16 cycles (14 - 19)	16 (14 - 19)?
<b>Integer ALUs</b>	4	4
<b>Load/Store Units</b>	2	2
<b>Addition (FP) Latency</b>	5 cycles	4 cycles
<b>Multiplication (INT) Latency</b>	4 cycles	3 cycles
<b>Branch Units</b>	2	2
<b>Indirect Branch Units</b>	1	1
<b>FP/NEON ALUs</b>	3	3
<b>L1 Cache per core</b>	64KB I\$ + 64KB D\$	64KB I\$ + 64KB D\$
<b>L2 Cache per core</b>	1MB	1MB
<b>L3 Cache (shared)</b>	4MB	4MB



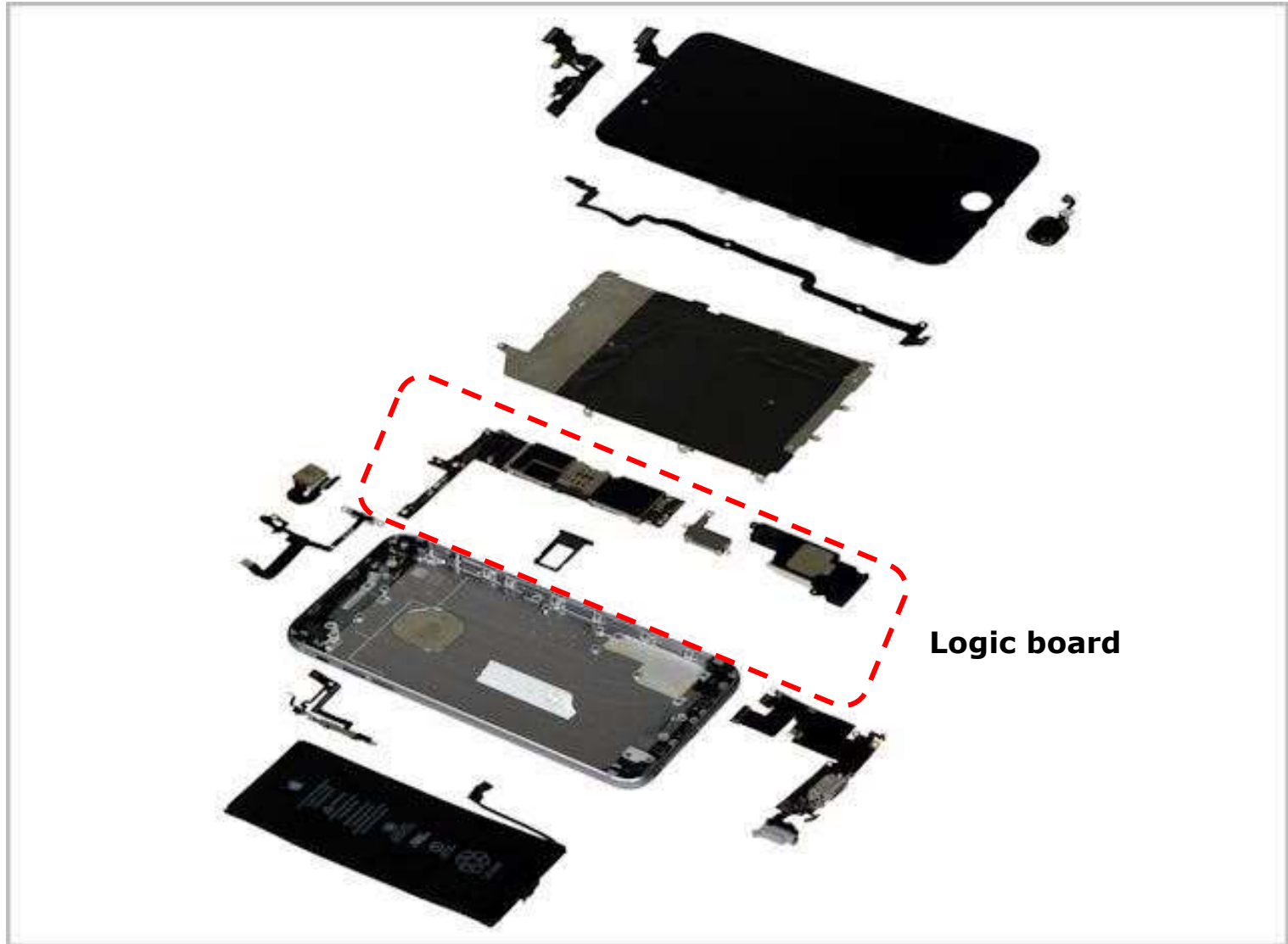
## 6. Apple A8 with dual Typhoon cores (8)

### Layout of the Typhoon core of the A8

- Despite the fact that A8's Typhoon core has basically the same microarchitecture as A7's Cyclone core, its transistor count is raised from about 1 billion to about 2 billion.
- This astonishing doubling of the transistor count may result from the fact that the A8 is a complete redesign of the A7 on a new process technology of TSMC while focusing on raising the energy efficiency.
- Actually, Apple declared that the A8 is up to 50 % more energy efficient than the A7.

## 6. Apple A8 with dual Typhoon cores (9)

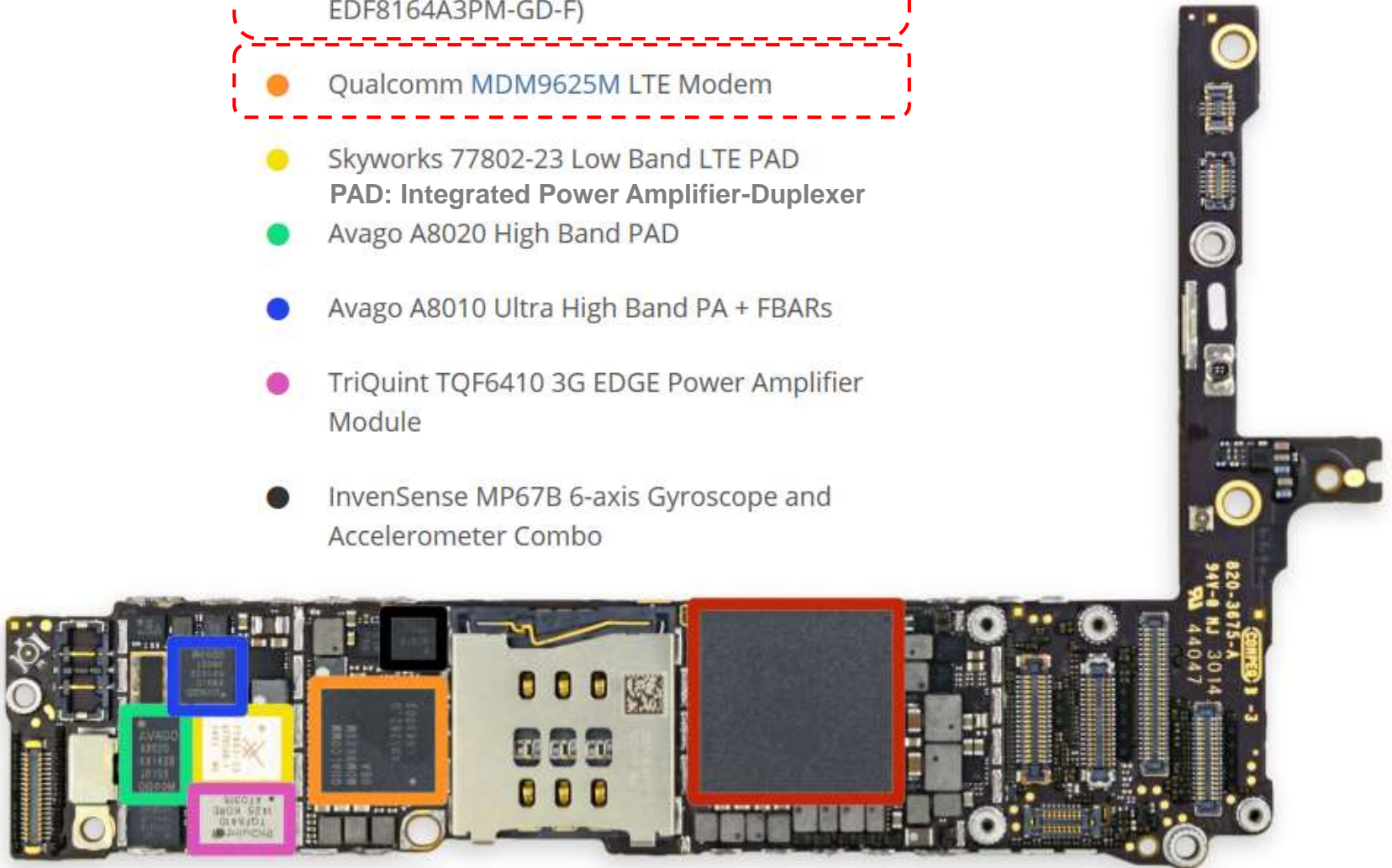
Exploded assembly drawing of the iPhone 6+ [30]



## 6. Apple A8 with dual Typhoon cores (10)

The front side of the logic board of the iPhone 6+ [31]-1

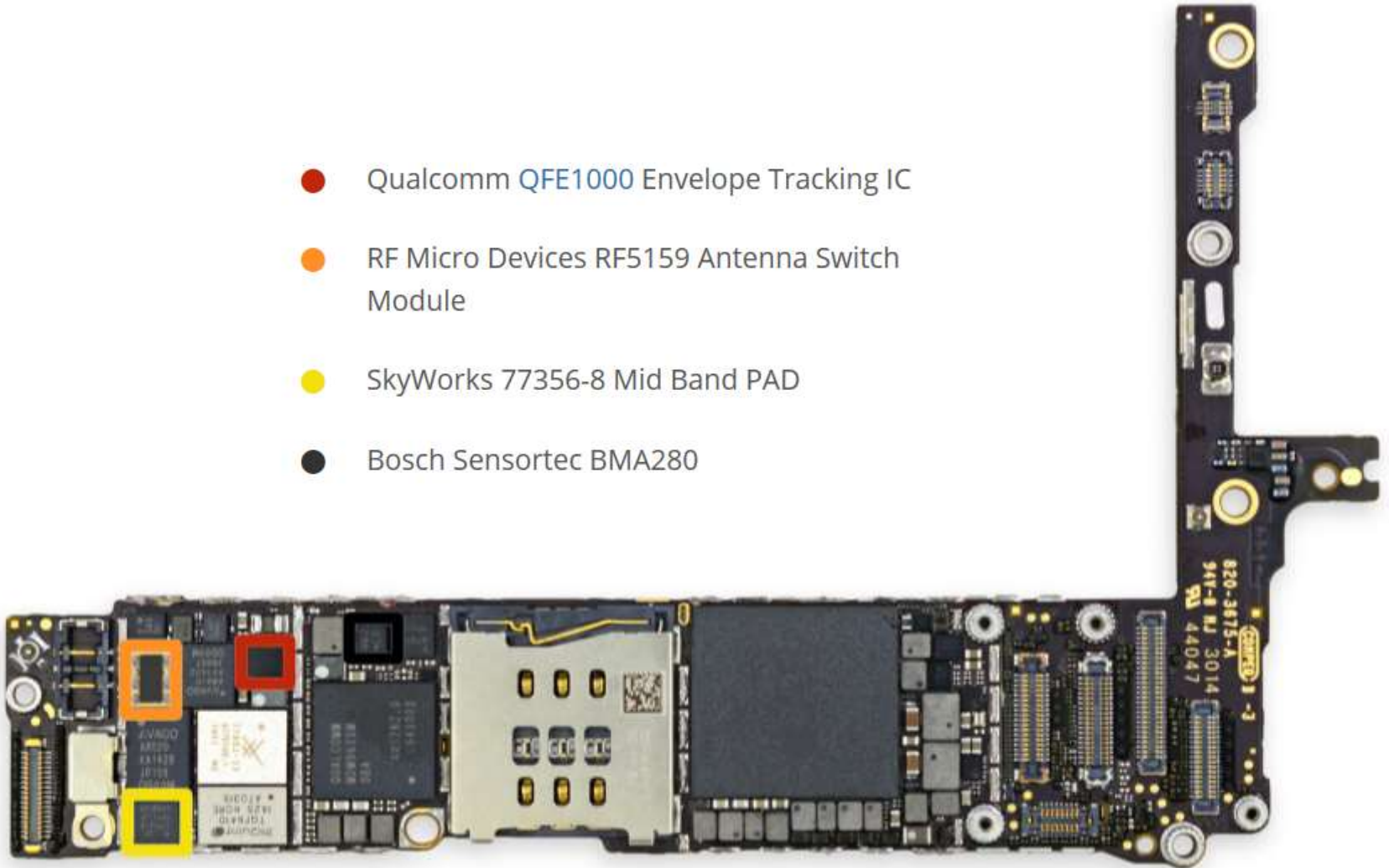
- Apple A8 APL1011 SoC + Elpida 1 GB LPDDR3 RAM (as denoted by the markings EDF8164A3PM-GD-F)
- Qualcomm MDM9625M LTE Modem
- Skyworks 77802-23 Low Band LTE PAD  
**PAD: Integrated Power Amplifier-Duplexer**
- Avago A8020 High Band PAD
- Avago A8010 Ultra High Band PA + FBARs
- TriQuint TQF6410 3G EDGE Power Amplifier Module
- InvenSense MP67B 6-axis Gyroscope and Accelerometer Combo



## 6. Apple A8 with dual Typhoon cores (11)

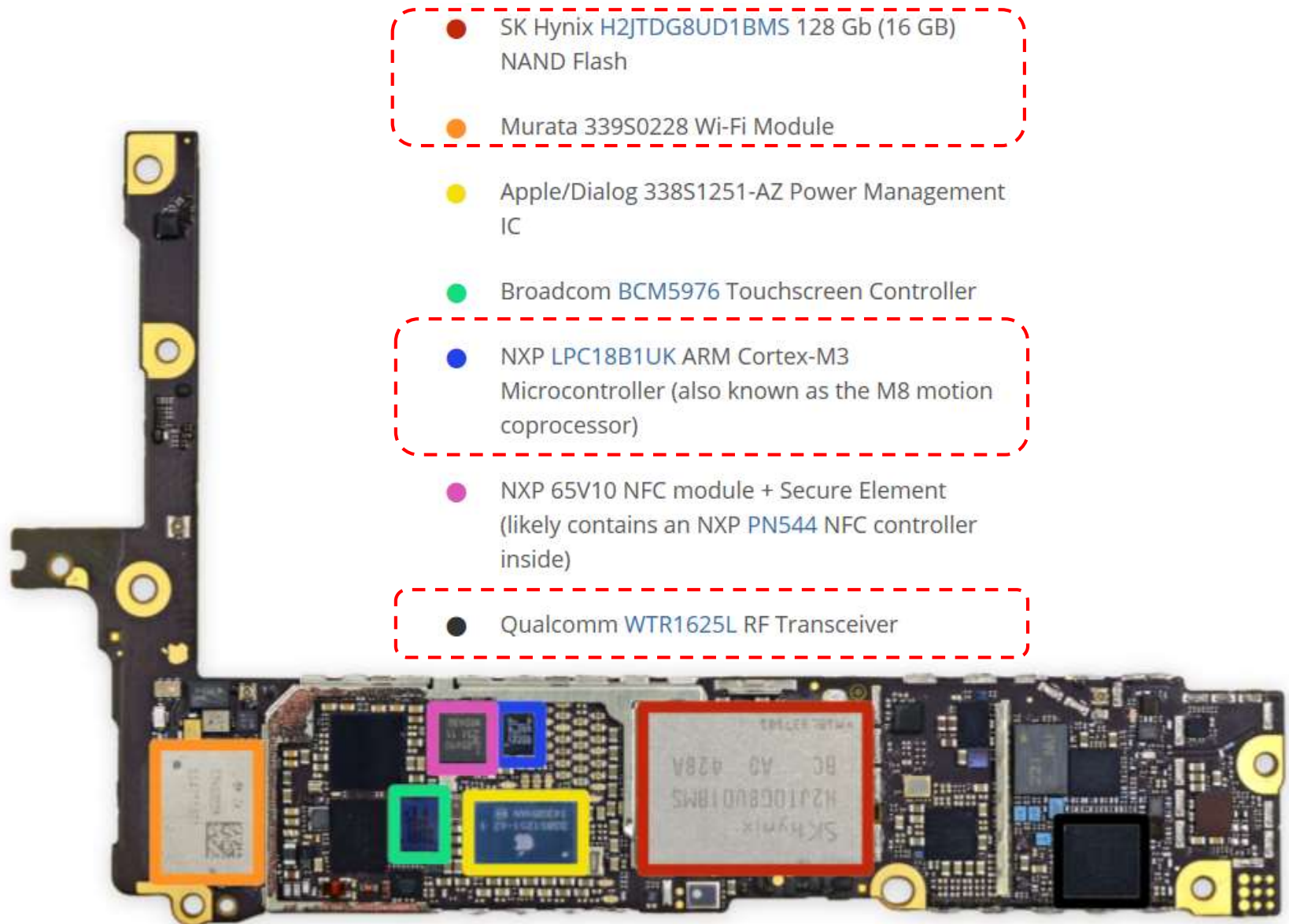
The front side of the logic board of the iPhone 6+ [31]-2

- Qualcomm QFE1000 Envelope Tracking IC
- RF Micro Devices RF5159 Antenna Switch Module
- SkyWorks 77356-8 Mid Band PAD
- Bosch Sensortec BMA280



## 6. Apple A8 with dual Typhoon cores (12)

The back side of the logic board of the iPhone 6+ [31]-1

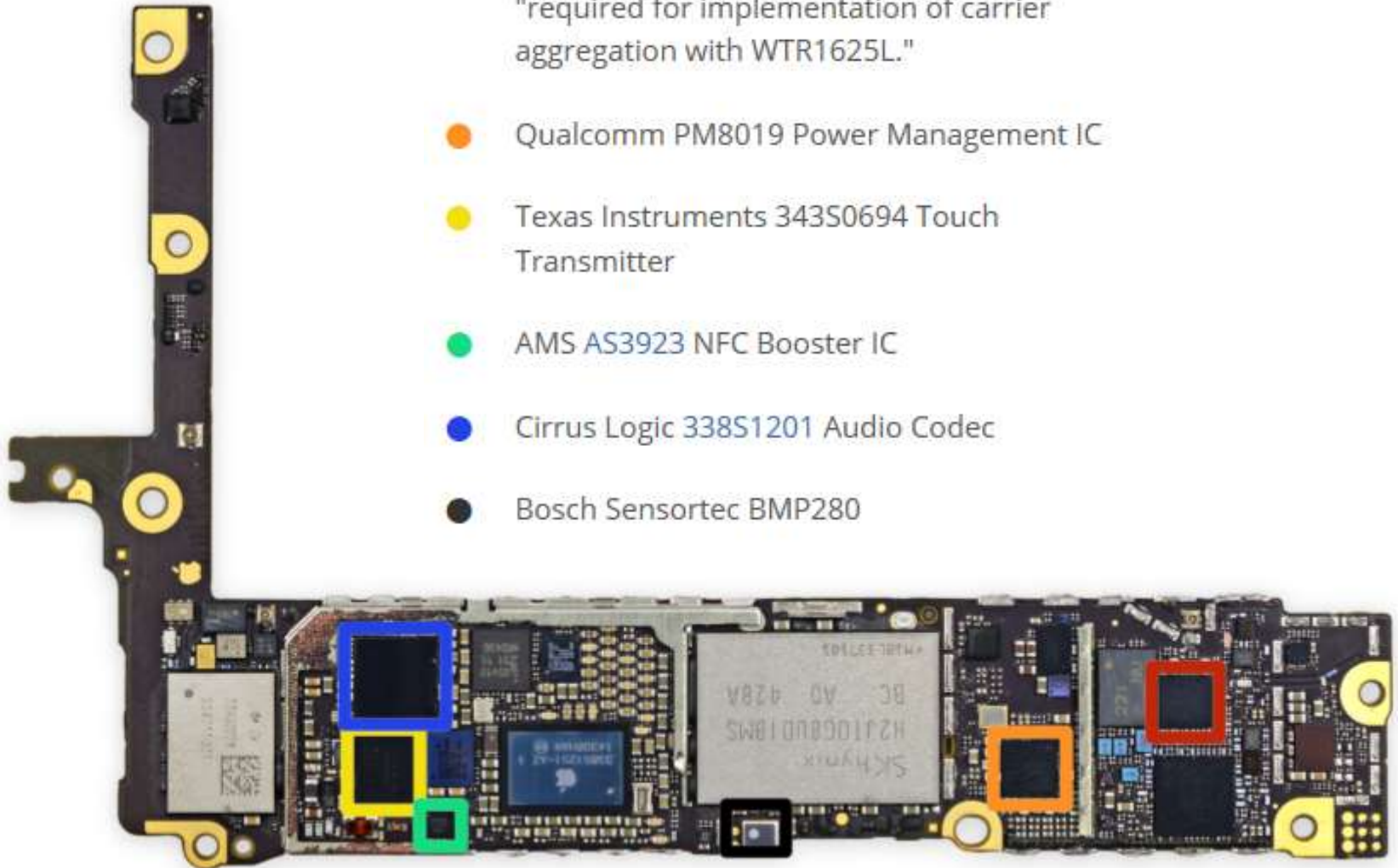




## 6. Apple A8 with dual Typhoon cores (13)

The back side of the logic board of the iPhone 6+ [31]-2

- Qualcomm WFR1620 receive-only companion chip. Qualcomm [states](#) that the WFR1620 is "required for implementation of carrier aggregation with WTR1625L."
- Qualcomm PM8019 Power Management IC
- Texas Instruments 343S0694 Touch Transmitter
- AMS AS3923 NFC Booster IC
- Cirrus Logic 338S1201 Audio Codec
- Bosch Sensortec BMP280



## 7. Apple A8X with triple Typhoon cores








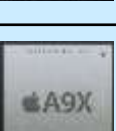
## 7. Apple A8X with triple Typhoon cores (1)

### 7. Apple A8X with triple Typhoon cores

- The **A8X** emerged along with the iPad Air 2 in 10/2014.
- It has **three Typhoon cores** rather than two as in the A8 SoC.
- Furthermore, it has an enhanced GPU in comparison to the A8.

## 7. Apple A8X with triple Typhoon cores (2)

### Main features of the A8X

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A7</b>	APL0698 or S5L8960		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.3 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2013	iPhone 5S iPad Mini 2 iPad Mini 3
	APL5698 or S5L8965		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	10/2013	iPad Air 9.7"
<b>A8</b>	APL1011		20 nm HKMG	89 mm <sup>2</sup>	2x Typhoon 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR GX6450 (4C) @ 450 MHz (115.2 GFLOPS)	1GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2014	iPhone 6 iPhone 6 Plus
<b>A8X</b>	APL1012		20 nm HKMG	128 mm <sup>2</sup>	3xTyphoon 1.5 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 2 MB L3: 4 MB	PowerVR GX6850 (5C) @ 450 MHz (230.4 GFLOPS)	2 GB 64-bit DCh LPDDR3-1600 (25.6 GB/sec)	10/2014	iPad Air 2 9.7"
<b>A9</b>	APL1022 (TSMC) APL0898 (Samsung)		16 nm FinFET 14 nm FinFET	104.5 mm <sup>2</sup>	2xTwister 1.85 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: 4 MB	PowerVR GT7600 (6C) @ 450 MHz (172.8 GFLOPS)	2 GB 64-bit SCh LPDDR4-3200 (25.6 GB/sec)	9/2015	iPhone 6s iPhone 6s Plus iPhone SE
<b>A9X</b>	APL1021 (TSMC)		16 nm FinFET	147 mm <sup>2</sup>	2xTwister 2.16-2.26 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: none	PowerVR 7XT series (12C) @ n.a. MHz (345.6 GFLOPS)	2 GB/4 GB 64-bit DCh LPDDR4-3200 (51.2 GB/sec)	11/2015 (12.9") 3/2016 (9.7")	iPad Pro 9.7" iPad Pro 12.9"

## 7. Apple A8X with triple Typhoon cores (3)

Main features of the A8X compared to the Apple A8 [32]

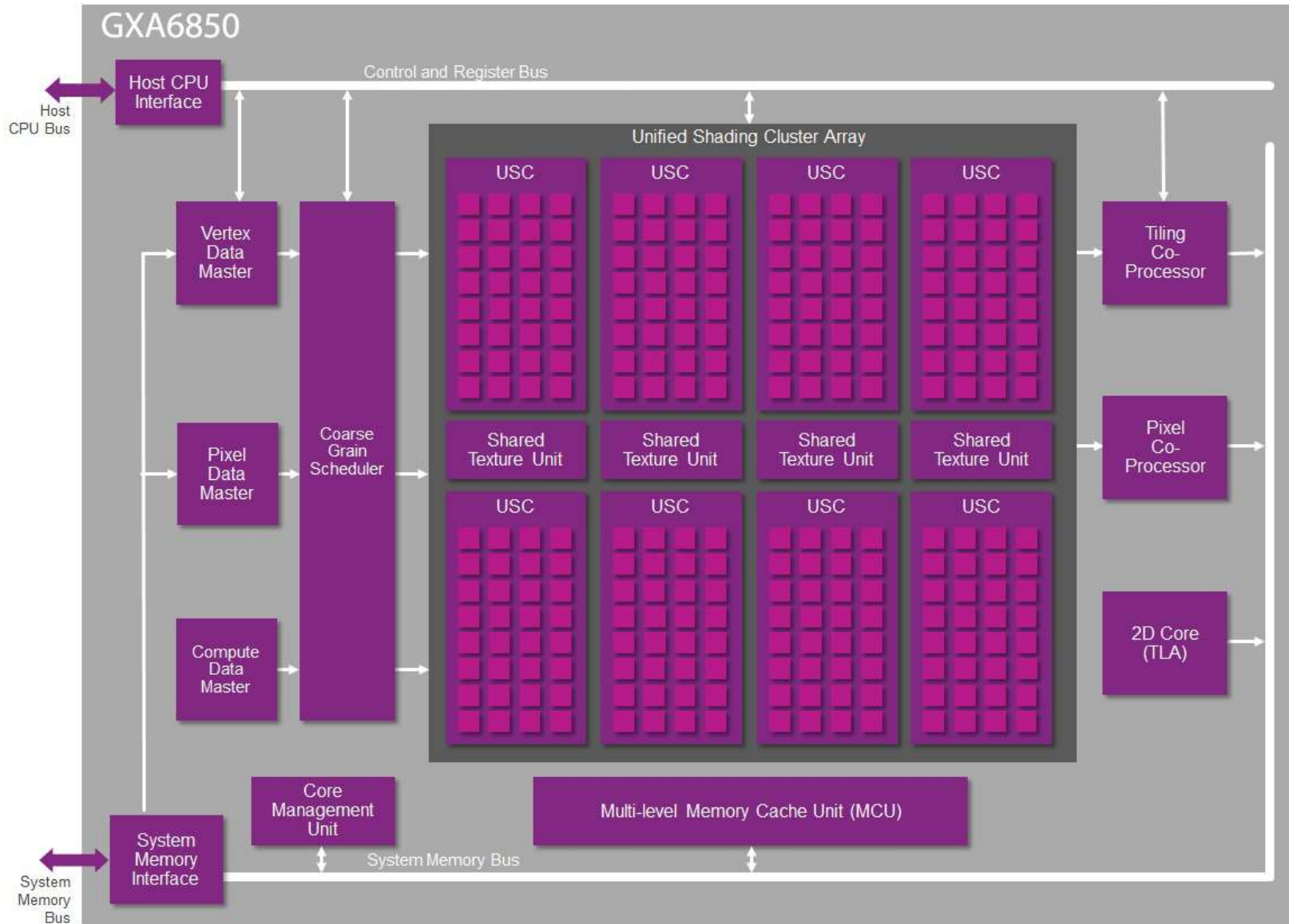
Apple SoC Comparison				
	A8X	A8	A7	A6X
<b>CPU</b>	3x "Enhanced Cyclone"	2x "Enhanced Cyclone"	2x Cyclone	2x Swift
<b>CPU Clockspeed</b>	1.5GHz	1.4GHz	1.4GHz (iPad)	1.3GHz
<b>GPU</b>	Apple/PVR GXA6850	PVR GX6450	PVR G6430	PVR SGX554 MP4
<b>RAM</b>	2GB	1GB	1GB	1GB
<b>Memory Bus Width</b>	128-bit	64-bit	64-bit	128-bit
<b>Memory Bandwidth</b>	25.6GB/sec	12.8GB/sec	12.8GB/sec	17.1GB/sec
<b>L2 Cache</b>	2MB	1MB	1MB	1MB
<b>L3 Cache</b>	4MB	4MB	4MB	N/A
<b>Transistor Count</b>	~3B	~2B	>1B	N/A
<b>Manufacturing Process</b>	TSMC(?) 20nm	TSMC 20nm	Samsung 28nm	Samsung 32nm

## 7. Apple A8X with triple Typhoon cores (4)

- Further enhancement of the A8X vs. the A8 SOC, not mentioned in the above Table [32]
- The [GXA6850 GPU of the A8X has 8 cores](#) rather than only 4, as in case of the GX6450 GPU of the A8 (see next Figure).

## 7. Apple A8X with triple Typhoon cores (5)

The GXA6850 GPU of the AX8-1 [32]



## 7. Apple A8X with triple Typhoon cores (6)

The GXA6850 GPU of the AX8 -2 [33]

- Each of the 8 graphics cores of the GXA6850 (called USC in the above Figure) includes 32 FP32 ALUs.
- Consequently, the 8 graphics cores have altogether 256 FP32 ALUs.
- Each ALU can perform 2 operations per cycle, thus the GXA6850 can execute  $256 \times 2 = 512$  operations/cycle.
- At an assumed clock rate of 450 MHz this results in 230 GFLOPS, a value that exceeds by a small margin the FP performance of NVIDIA's K1.

## 7. Apple A8X with triple Typhoon cores (7)

Implementing the DRAM memory in form of two external chips [27]

Apple implemented the larger (2 GB) DRAM memory of the A8X in form of two external memory chips mounted onto the PC board on both sides of the A8X chip, rather than as stacked memory as in previous designs, as seen below.

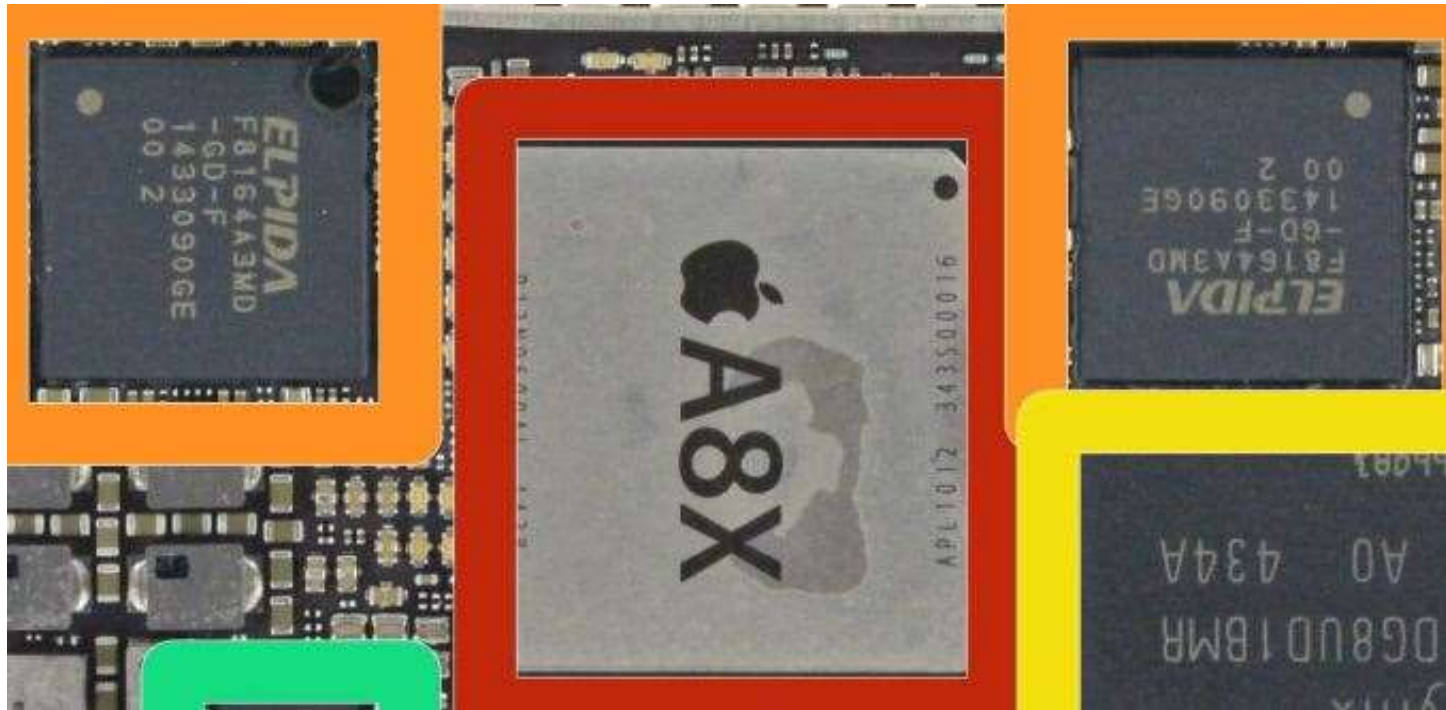
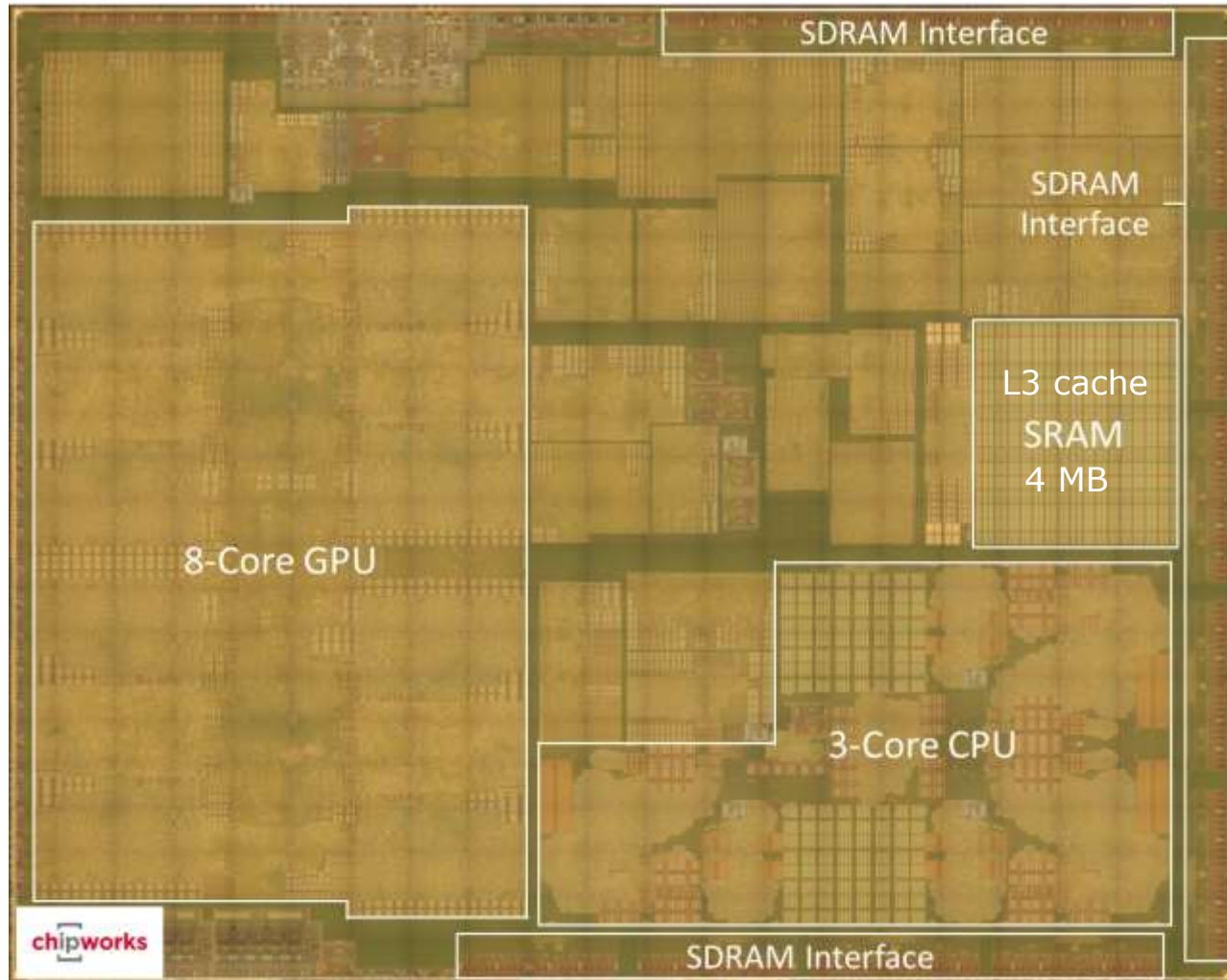


Figure: ELPIDA DRAM chips mounted onto the PC board on both sides of the A8X [27]



## 7. Apple A8X with triple Typhoon cores (8)

Die plot of the A8X [32]

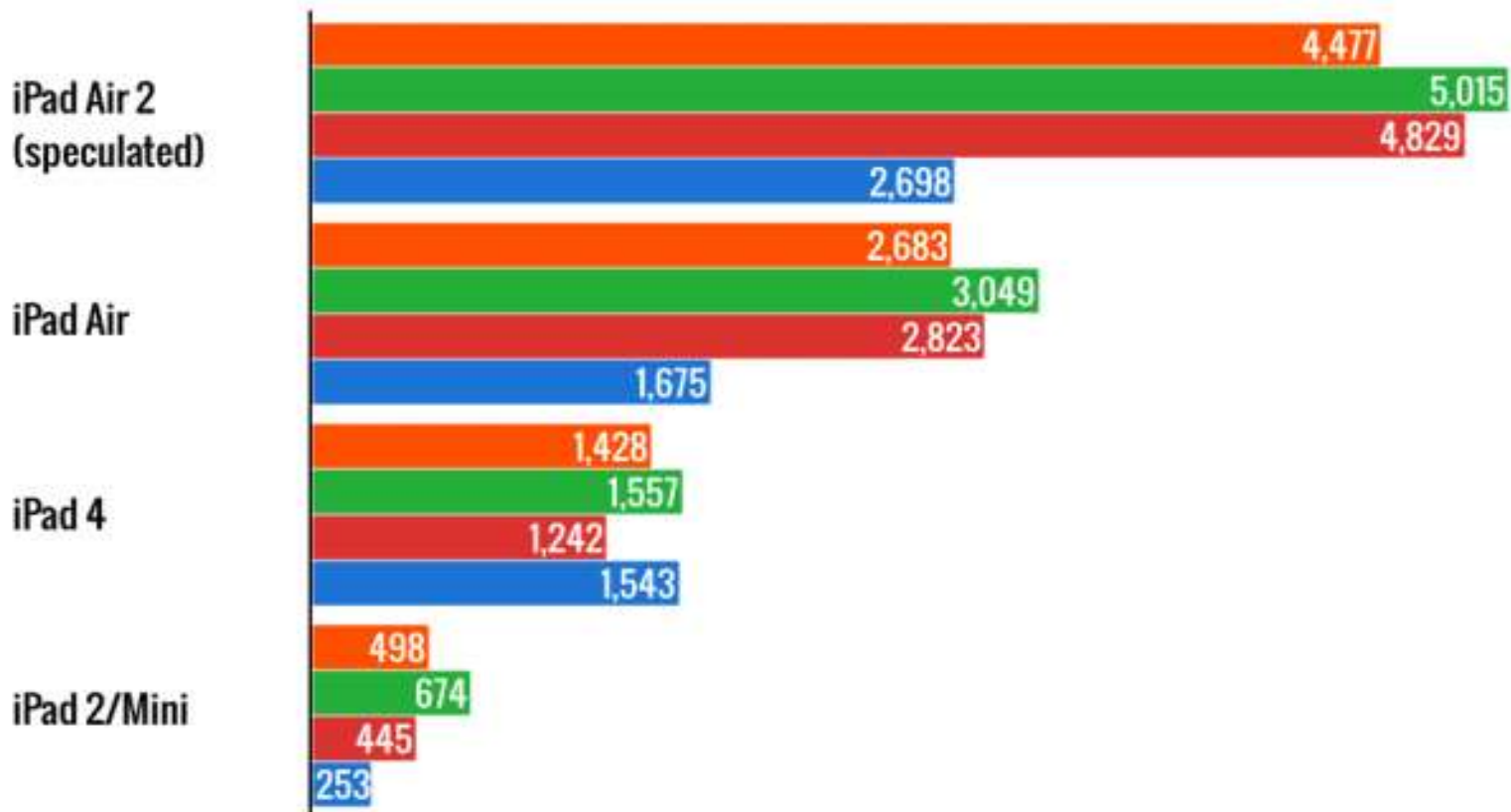


## 7. Apple A8X with triple Typhoon cores (9)

Performance of the iPad Air 2 vs. previous iPad models measured using the Geekbench 3.2 benchmark [34]

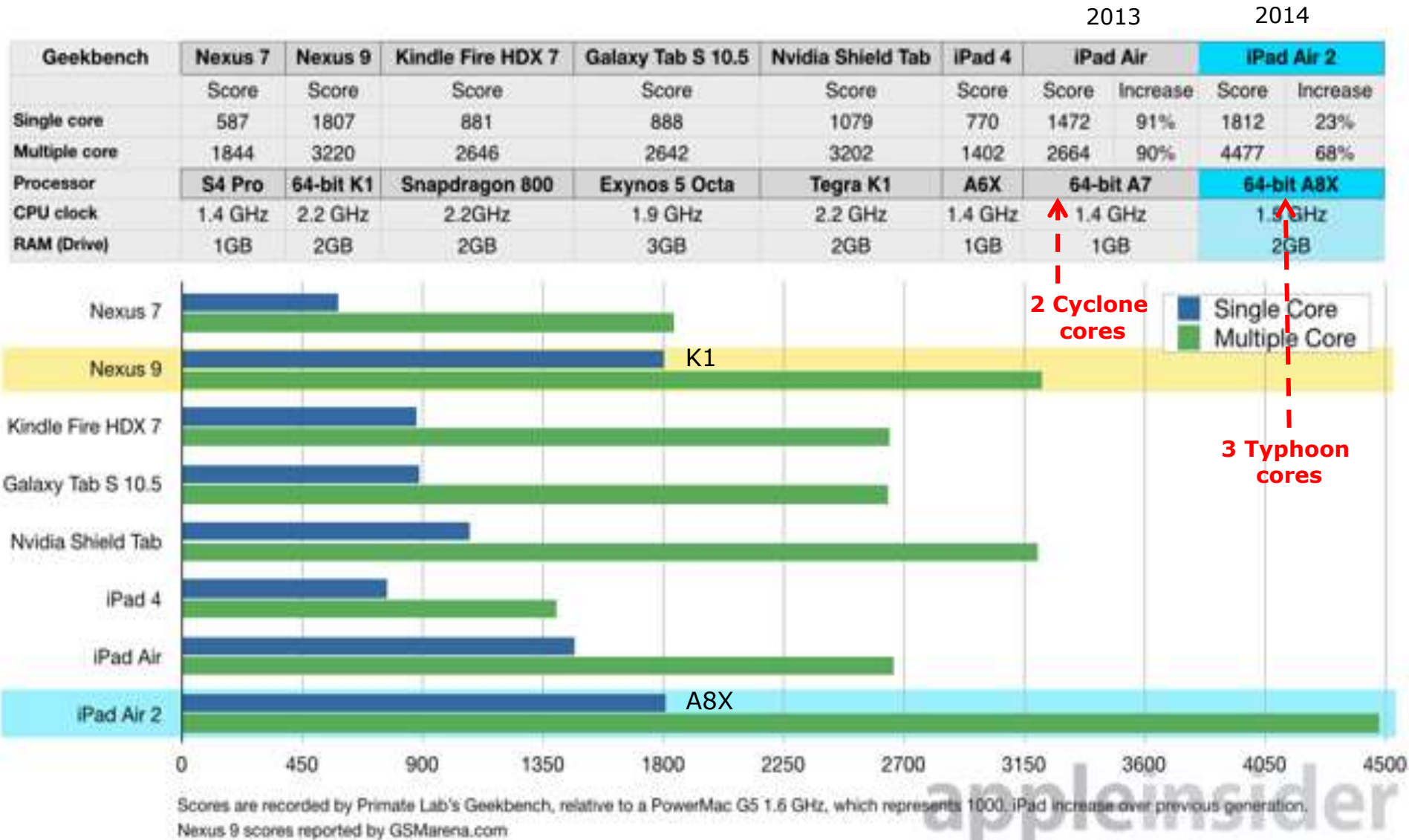
### GEEKBENCH 3.2: MULTI-CORE (Higher is better)

Overall Floating point  
Integer Memory



## 7. Apple A8X with triple Typhoon cores (10)

Performance of the iPad Air 2 vs. competing models measured using the Geekbench 3.2 benchmark [35]



## 7. Apple A8X with triple Typhoon cores (11)

Implications of the extremely high performance of Apple's A8X-based iPad Air 2 (including 3 Typhoon cores) [50] -1

- **Intel** lost Apple as a perspective buyer of their chips for the iPad line, and the iPad Air 2 also severely hit the perspective of their not so successful Atom line.
- Intel tried to raise their market share on the mobile market by paying subsidies to OEMs who were buying Atom processors, but due to their high losses suffered Intel first stopped paying subsidies and then in 4/2016 the firm announced their withdrawal from the mobile market.
- **NVIDIA's** Tegra 4 chips were not successful as well, so the firm announced in 05/2014 that they will abandon the phone market.

Apple's iPad Air 2 with its A8X processor and its GPU with 256 EUs became a very powerful rival to NVIDIA's subsequent 64-bit K1 chip including a GPU with 192 EUs.

As a consequence, **NVIDIA** also gave up their tablet interests.

## 7. Apple A8X with triple Typhoon cores (12)

### Implications of the extremely high performance of Apple's A8X-based iPad Air 2 (including 3 Typhoon cores) -2

- **NVIDIA's** Tegra 4 chips were not successful as well, so **the firm announced in 05/2014 that they will abandon the phone market.**
- Apple's iPad Air 2 with its A8X processor and its GPU with 256 EUs became a very powerful rival to NVIDIA's subsequent 64-bit K1 chip including a GPU with 192 EUs.
- As a consequence, in 6/2016 (at Computex) NVIDIA's CEO declared the firm's leaving both the smartphone and tablet market by saying [61]:  
: **"We are no longer interested in that market". He adds, "Anybody can build smartphones, and we're happy to enjoy these devices, but we'll let someone else build them".**
- Instead NVIDIA became interested in designing in-car computers and car infotainment systems.

## 7. Apple A8X with triple Typhoon cores (13)

Implications of the extremely high performance of Apple's A8X-based iPad Air 2 (including 3 Typhoon cores) [36] -3

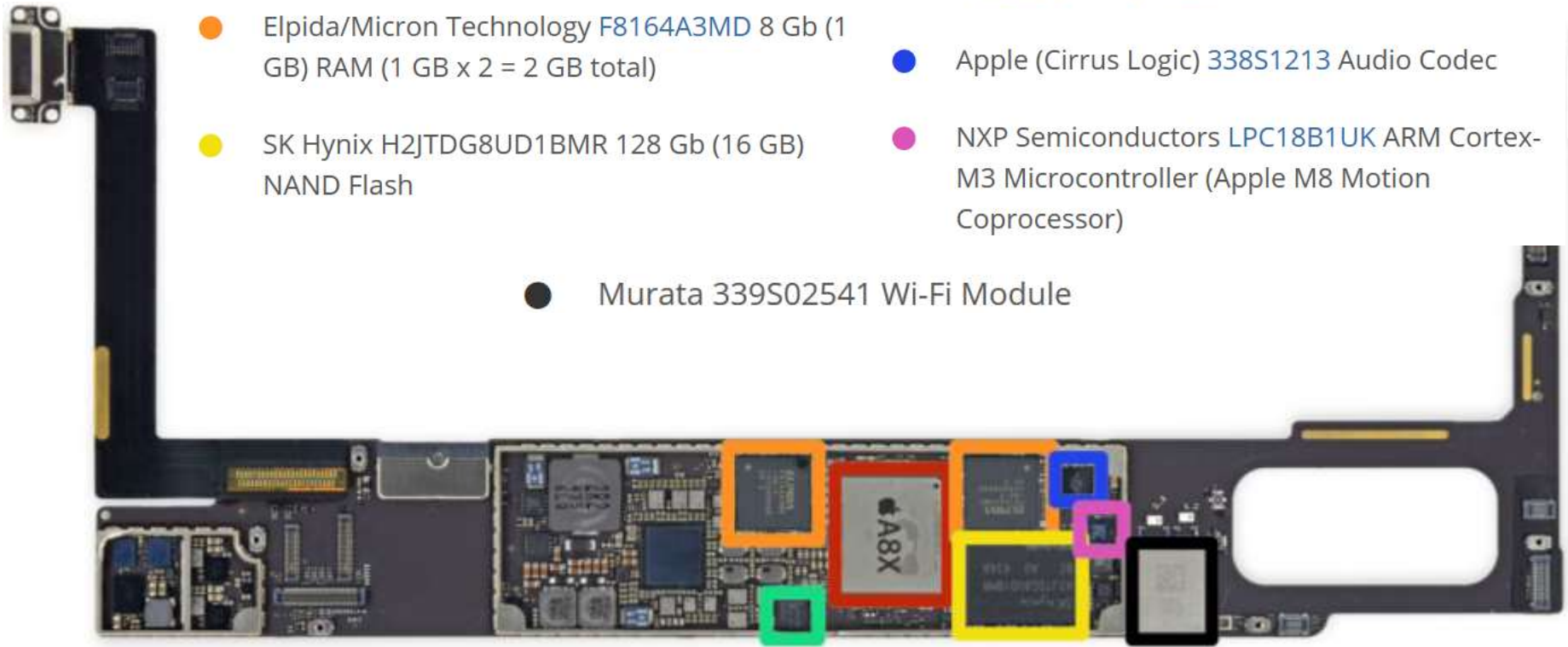
- **Texas Instruments (TI) OMAP family is used in** Kindle Fire and a variety of Samsung's Galaxy Tab models.
- TI however **failed to compete successfully against Apple** so was forced to announce a major shift in its business strategy in 9/2012, by **leaving the consumer application processor business** entirely and **focusing on embedded applications**, such as using processors in cars.



## 7. Apple A8X with triple Typhoon cores (14)

### iPad Air 2 board with main components [37]

- Apple APL1012 A8X 64-bit Processor
- Elpida/Micron Technology F8164A3MD 8 Gb (1 GB) RAM (1 GB x 2 = 2 GB total)
- SK Hynix H2JTDG8UD1BMR 128 Gb (16 GB) NAND Flash
- NXP 65V10 NFC Controller (as found in the iPhone 6 and 6 Plus)
- Apple (Cirrus Logic) 338S1213 Audio Codec
- NXP Semiconductors LPC18B1UK ARM Cortex-M3 Microcontroller (Apple M8 Motion Coprocessor)
- Murata 339S02541 Wi-Fi Module





## 8. Apple A9 with dual Twister cores

### 8. Apple A9 with dual Twister cores [42]

- The A9 emerged in the mobile devices
  - iPhone 6s and
  - iPhone 6s Plusin 9/2015.
- It is dual sourced, Samsung fabricates the A8 in the 16 nm FinFET technology whereas TSMC in the 14 nm technology.
- Apple did not reveal a transistore count for the A9.
- The clock rate of the A9 has considerable increased vs. the A8, from 1.4 GHz to 1.85 GHz.
- Apple states that the A9 has 70% higher CPU performance and 90% more graphics performance than its predecessor, the A8 [42].







## 8. Apple A9 with dual Twister cores (2)

Contrasting key components of the A9 vs. the A8 [40]

	Apple A9 (2015)	Apple A8 (2014)
<b>Manufacturing Process</b>	TSMC 16nm FinFET / Samsung 14nm FinFET	TSMC 20nm HKMG
<b>Die Size</b>	104.5mm <sup>2</sup> /96mm <sup>2</sup>	89mm <sup>2</sup>
<b>CPU</b>	2 x Apple Twister ARMv8 64-bit cores	2 x Apple Typhoon ARMv8 64-bit cores
<b>GPU</b>	IMG PowerVR GT7600	IMG PowerVR GX6450

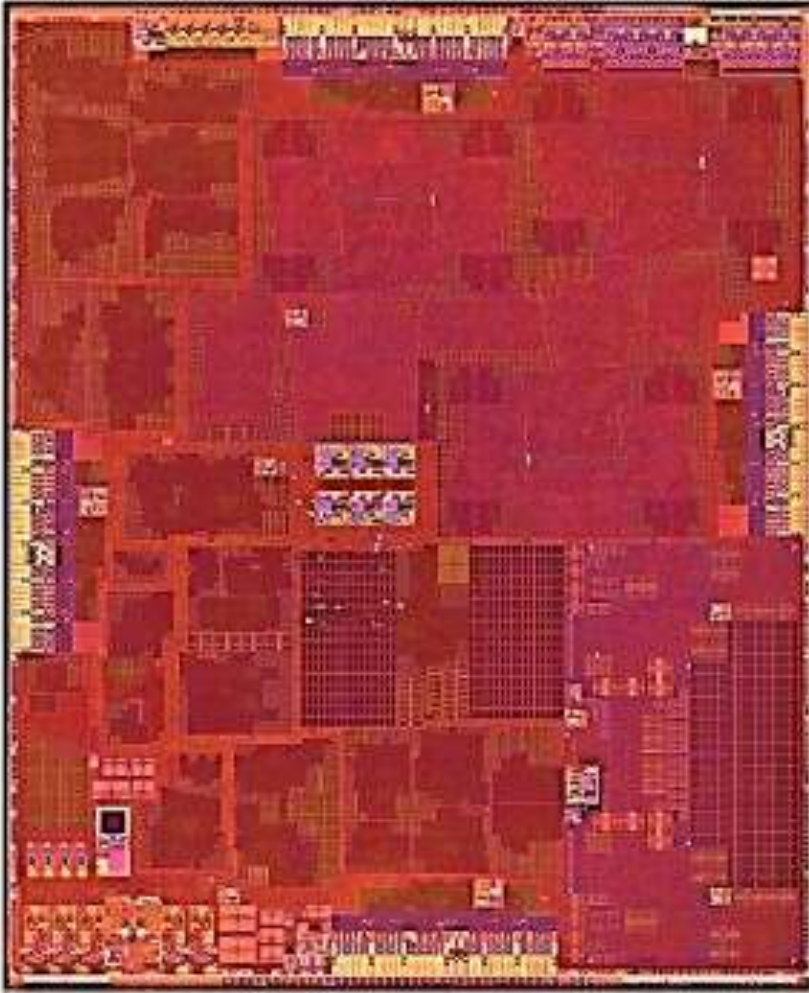
## 8. Apple A9 with dual Twister cores (3)

### Main features of the A9

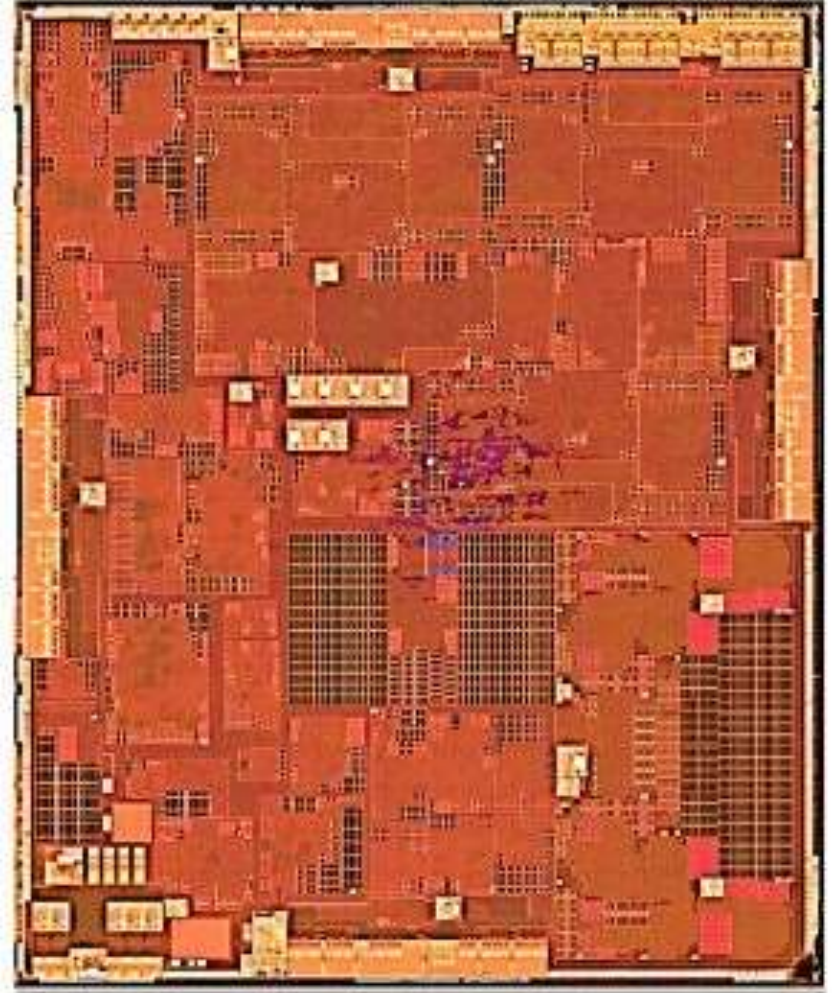
Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A7</b>	APL0698 or S5L8960		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.3 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2013	iPhone 5s iPad Mini 2 iPad Mini 3
	APL5698 or S5L8965		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	10/2013	iPad Air
<b>A8</b>	APL1011		20 nm HKMG	89 mm <sup>2</sup>	2x Typhoon 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR GX6450 (4C) @ 450 MHz (115.2 GFLOPS)	1GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2014	iPhone 6 iPhone 6 Plus
<b>A8X</b>	APL1012		20 nm HKMG	128 mm <sup>2</sup>	3xTyphoon 1.5 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 2 MB L3: 4 MB	PowerVR GX6450 (5C) @ 450 MHz (230.4 GFLOPS)	2 GB 64-bit DCh LPDDR3-1600 (25.6 GB/sec)	10/2014	iPad Air 2
<b>A9</b>	APL1022 (TSMC) APL0898 (Samsung)		16 nm FinFET 14 nm FinFET	104.5 mm <sup>2</sup>	2xTwister 1.85 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: 4 MB	PowerVR GT7600 (6C) @ 450 MHz (172.8 GFLOPS)	2 GB 64-bit SCh LPDDR4-3200 (25.6 GB/sec)	9/2015	iPhone 6s iPhone 6s Plus iPhone SE
<b>A9X</b>	APL1021 (TSMC)		16 nm FinFET	147 mm <sup>2</sup>	2xTwister 2.16-2.26 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: none	PowerVR 7XT series (12C) @ n.a. MHz (345.6 GFLOPS)	2 GB/4 GB 64-bit DCh LPDDR4-3200 (51.2 GB/sec)	11/2015 (12.9") 3/2016 (9.7")	iPad Pro 9.7" iPad Pro 12.9"

## 8. Apple A9 with dual Twister cores (4)

Contrasting the alternative implementations of A9 [40]



APL1022 – TSMC 16 nm FinFET



APL0898 – Samsung 14 nm FinFET

## 8. Apple A9 with dual Twister cores (5)

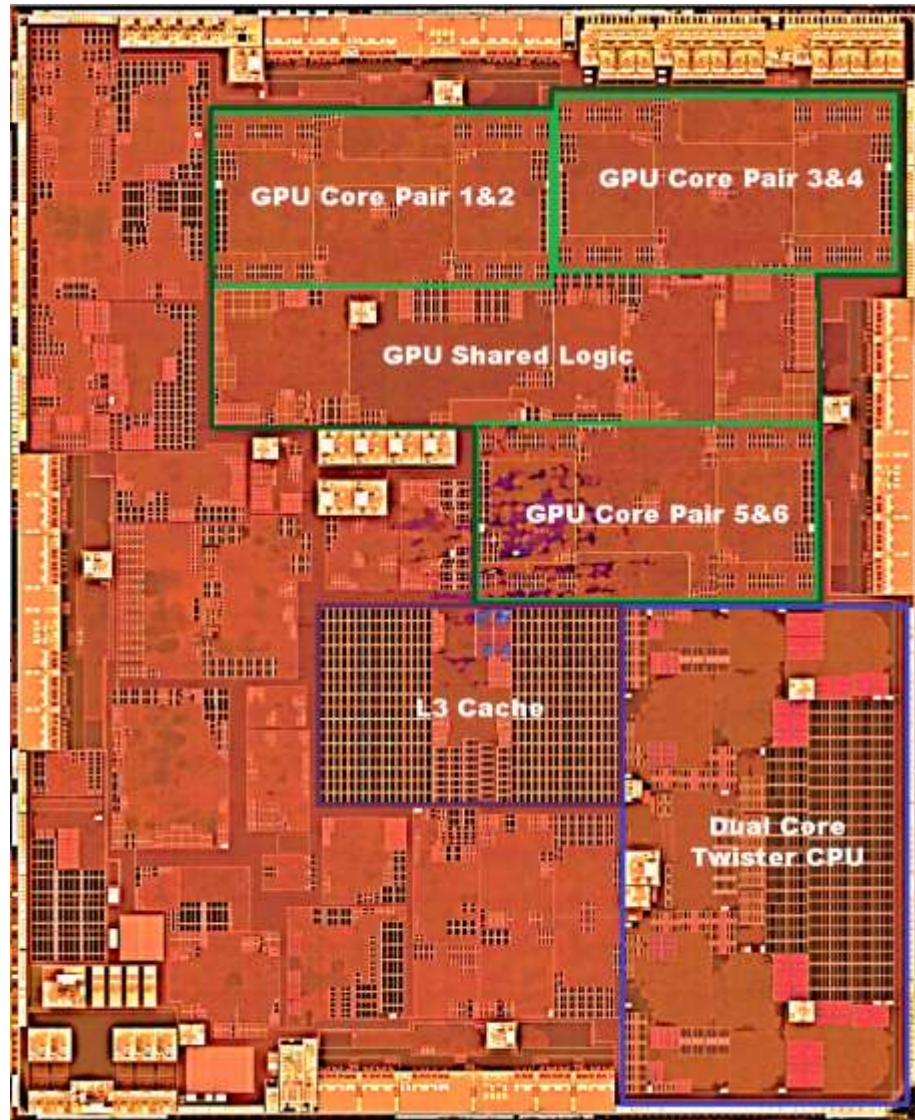
Evolution of the microarchitectures of the A line from the A7 to A9X [41]

	A9X	A9	A8	A7
<b>CPU</b>	2x Twister	2x Twister	2x Typhoon	2x Cyclone
<b>CPU Clockspeed</b>	2.26GHz	1.85GHz	1.4GHz	1.3GHz
<b>GPU</b>	PVR 12 Cluster Series7	PVR GT7600	PVR GX6450	PVR G6430
<b>RAM</b>	4GB LPDDR4	2GB LPDDR4	1GB LPDDR3	1GB LPDDR3
<b>Memory Bus Width</b>	128-bit	64-bit	64-bit	64-bit
<b>Memory Bandwidth</b>	51.2GB/sec	25.6GB/sec	12.8GB/sec	12.8GB/sec
<b>L2 Cache</b>	3MB (shared)	3MB (shared)	1MB (shared)	1MB (shared)
<b>L3 Cache</b>	None	4MB (Victim)	4MB (Inclusive)	4MB (Inclusive)
<b>Manufacturing Process</b>	TSMC 16nm FinFET	TSMC 16nm & Samsung 14nm	TSMC 20nm	Samsung 28nm



## 8. Apple A9 with dual Twister cores (6)

Die plot of the A9 including dual Twister cores [41]





## 8. Apple A9 with dual Twister cores (7)

Contrasting key features of the microarchitectures of the A8 and A7 [40]

	Apple A8	Apple A9
<b>CPU Codename</b>	Typhoon	Twister
<b>ARM ISA</b>	ARMv8-A (32/64-bit)	ARMv8-A (32/64-bit)
<b>Issue Width</b>	6 micro-ops	6 micro-ops
<b>Reorder Buffer Size</b>	192 micro-ops	192 micro-ops
<b>Branch Mispredict Penalty</b>	16 (14 - 19)	9
<b>Integer ALUs</b>	4	4
<b>Shifter ALUs</b>	2	4
<b>Load/Store Units</b>	2	2
<b>Addition (FP32) Latency</b>	4 cycles	3 cycles
<b>Multiplication (FP32) Latency</b>	5 cycles	4 cycles
<b>Addition (INT) Latency</b>	1 cycle	1 cycle
<b>Multiplication (INT) Latency</b>	3 cycles	3 cycles
<b>Branch Units</b>	2	2
<b>Indirect Branch Units</b>	1	1
<b>FP/NEON ALUs</b>	3 (3 Add or 2 Mult)	3 (3 Add or 3 Mult)
<b>L1 Cache</b>	64KB I\$ + 64KB D\$	64KB I\$ + 64KB D\$
<b>L2 Cache</b>	1MB (per core?)	3MB (shared)
<b>L3 Cache</b>	4MB (inclusive)	4MB (exclusive)

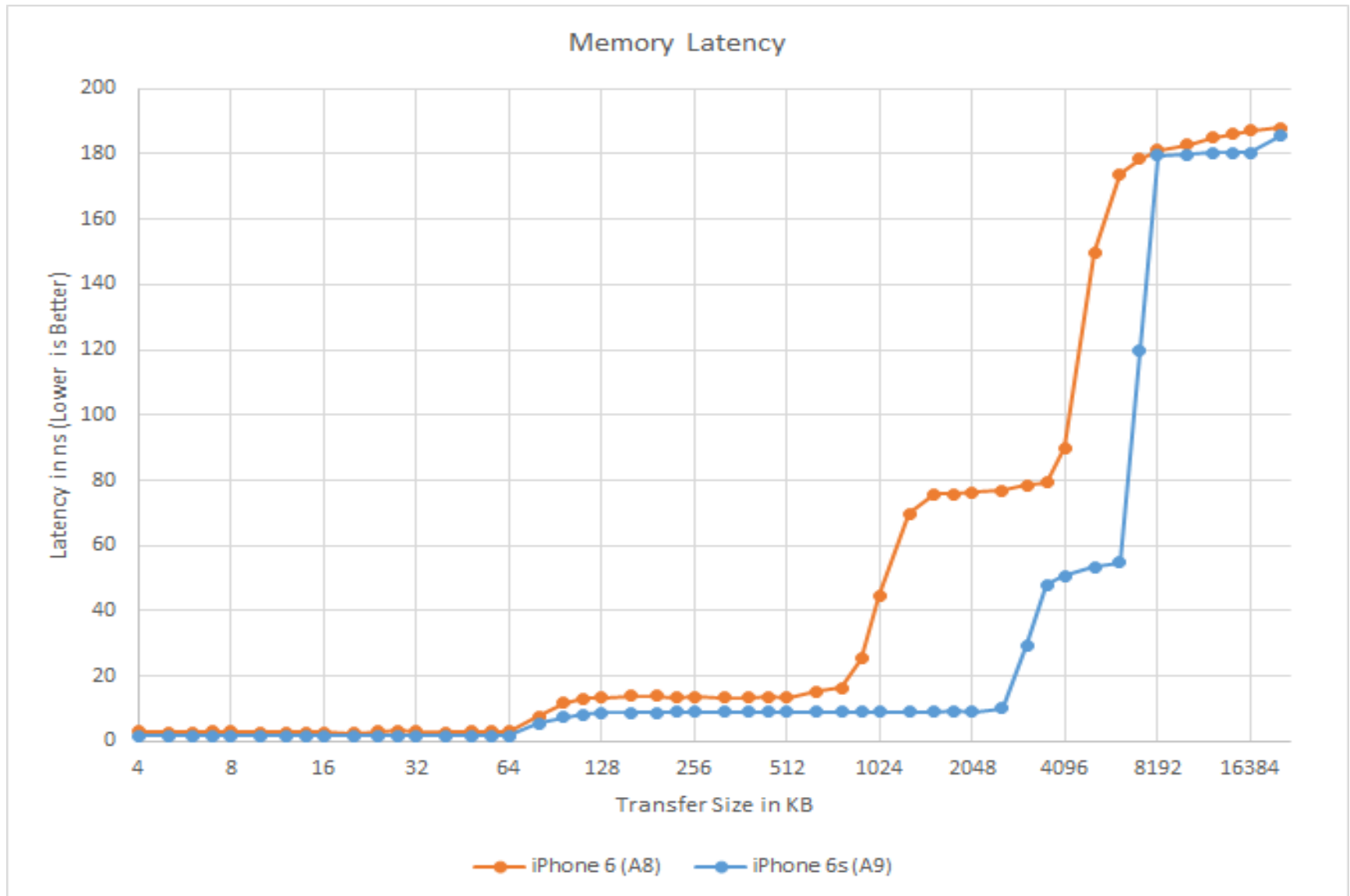
## 8. Apple A9 with dual Twister cores (8)

### Key differences between the microarchitectures of the A9 and the A8

- The A9 has
  - two more shifter **ALUs**
  - **faster 32-bit FP units** and
  - a redesigned L2 - L3 cache architecture.
- The **new cache architecture** means that in the A9
  - the **L2** cache became **shared** rather per core (as supposed to be in the A7) and
  - the **L3** cache became a **victim cache** rather than an inclusive cache,
  - as in the A7.
  - Further on the L2 and L3 caches provide in the **A9 shorter access times**, as seen in the next Figure.

## 8. Apple A9 with dual Twister cores (9)

Memory latency (ns) vs. transfer size (KB) of the A8 and A9 memory [41]



## 8. Apple A9 with dual Twister cores (10)

- **Note** that the L3 cache of the A8 became a victim cache (exclusive cache).

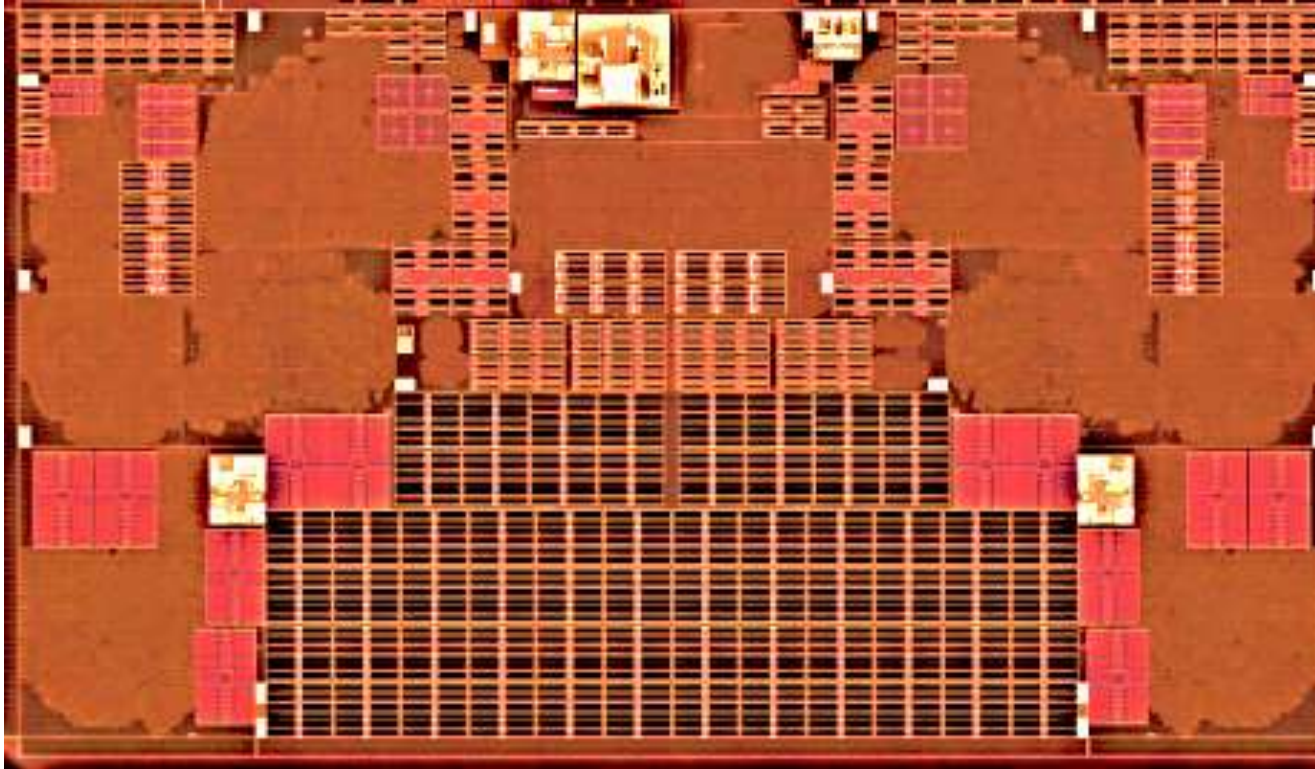
This means that recently used data that do not fit into the L2 cache and became evicted will be kept in the L3 cache, i.e. they remain still on-chip.

This improves performance and reduces power consumption.

- By reorganizing the L3 cache to a victim cache the 4 MB L3 cache of the A9 becomes more useful than an inclusive L3 that would hold the entire content of the 3 MB L2 cache and would leave only 1 MB space for other data [41].

## 8. Apple A9 with dual Twister cores (11)

Die micrograph of the dual core Twister CPU [40]



## 8. Apple A9 with dual Twister cores (12)

Integer performance increase (SPECint2000) of A9 vs. A8 [40]

SPECint2000 - Estimated Scores				
	A9	A8	% Advantage	% Architecture Advantage
<b>164.gzip</b>	1191	842	41%	9%
<b>175.vpr</b>	2017	1228	64%	32%
<b>176.gcc</b>	3148	1810	74%	42%
<b>181.mcf</b>	3124	1420	120%	88%
<b>186.crafty</b>	3411	2021	69%	37%
<b>197.parser</b>	1892	1129	68%	35%
<b>252.eon</b>	3926	1933	103%	71%
<b>253.perlbmk</b>	2768	1666	66%	34%
<b>254.gap</b>	2857	1821	57%	25%
<b>255.vortex</b>	3177	1716	85%	53%
<b>256.bzip2</b>	1944	1234	58%	25%
<b>300.twolf</b>	2020	1633	24%	-8

## 8. Apple A9 with dual Twister cores (13)

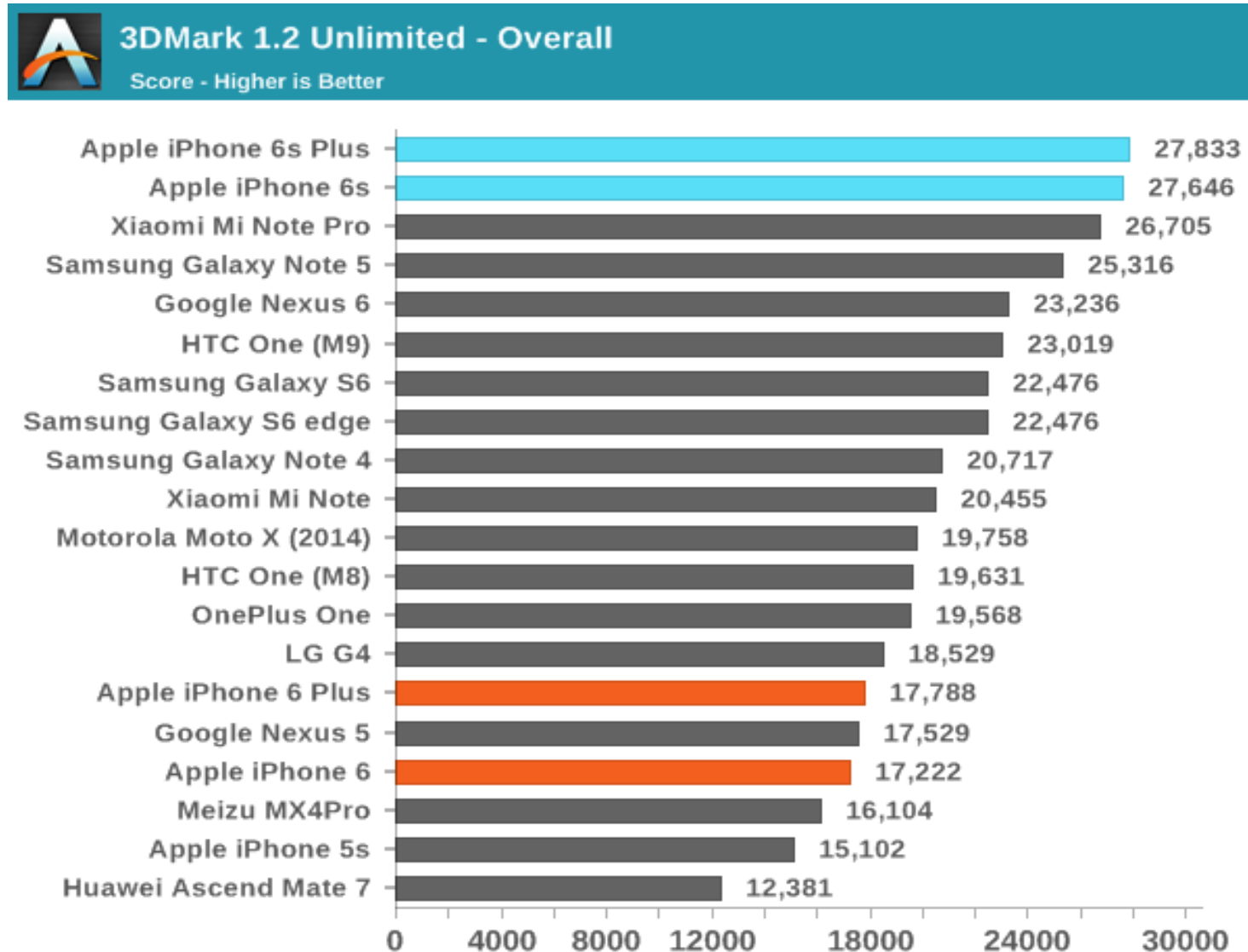
FP performance increase (Geekbench3) of A9 vs. A8 [40]

Geekbench 3 - Floating Point Performance				
	A9	A8	% Advantage	% Architecture Advantage
<b>BlackScholes ST</b>	11.9 Mnodes/s	7.85 Mnodes/s	52%	19%
<b>BlackScholes MT</b>	23.3 Mnodes/s	15.5 Mnodes/s	50%	18%
<b>Mandelbrot ST</b>	1.83 GFLOPS	1.18 GFLOPS	55%	23%
<b>Mandelbrot MT</b>	3.56 GFLOPS	2.34 GFLOPS	52%	20%
<b>Sharpen Filter ST</b>	1.69 MFLOPS	0.98 GFLOPS	72%	40%
<b>Sharpen Filter MT</b>	3.32 MFLOPS	1.94 MFLOPS	71%	39%
<b>Blur Filter ST</b>	2.22 GFLOPS	1.41 GFLOPS	57%	25%
<b>Blur Filter MT</b>	4.33 GFLOPS	2.78 GFLOPS	56%	24%
<b>SGEMM ST</b>	5.64 GFLOPS	3.83 GFLOPS	47%	15%
<b>SGEMM MT</b>	10.8 GFLOPS	7.48 GFLOPS	44%	12%
<b>DGEMM ST</b>	2.76 GFLOPS	1.87 GFLOPS	48%	15%
<b>DGEMM MT</b>	5.24 GFLOPS	3.61 GFLOPS	45%	13%
<b>SFFT ST</b>	2.83 GFLOPS	1.77 GFLOPS	60%	28%
<b>SFFT MT</b>	5.68 GFLOPS	3.47 GFLOPS	64%	32%
<b>DFFT ST</b>	2.64 GFLOPS	1.68 GFLOPS	57%	25%
<b>DFFT MT</b>	4.98 GFLOPS	3.29 GFLOPS	51%	19%
<b>N-Body ST</b>	1150 Kpairs/s	735.8 Kpairs/s	56%	24%
<b>N-Body MT</b>	2.27 Mpairs/s	1.46 Mpairs/s	55%	23%
<b>Ray Trace ST</b>	4.16 MP/s	2.76 MP/s	51%	19%
<b>Ray Trace MT</b>	8.15 MP/s	5.45 MP/s	50%	17%



## 8. Apple A9 with dual Twister cores (14)

Graphics performance (3DMark 1.2 Unlimited) of A9 vs. the competition [40]



## 9. Apple A9X with dual Twister cores

## 9. Apple A9X with dual Twister cores (1)

### 9. Apple A9X with dual Twister cores






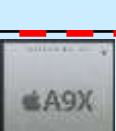
- The **A9X** appeared in the 12.9" iPad Pro (released in 11/2015) and then in the 9.7" iPad Pro version (released in 3/2016).

These models are designated as the **1. generation iPad Pro** models.

- **Key modifications vs. the A8X:**
  - Two Twister cores vs. three Typhoon cores
  - Much higher clock frequency (up to 2.26 GHz vs. 1.5 GHz)
  - Much higher memory speed (DDR4 with 3200 MT/s vs. DDR3 with 1600 MT/s)
  - 3 MB L2 without L3 vs. 2 MB L2 and 4 MB L3, and
  - higher performance graphics (12 graphics cores vs. 5).

## 9. Apple A9X with dual Twister cores (2)

### 9. Main features of the A9X

Appl. proc.	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A7</b>	APL0698 or S5L8960		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.3 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2013	iPhone 5S iPad Mini 2 iPad Mini 3
	APL5698 or S5L8965		28 nm HKMG	102 mm <sup>2</sup>	2x Cyclone 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR G6430 (4C) @ 450 MHz (115.2 GFLOPS)	1 GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	10/2013	iPad Air
<b>A8</b>	APL1011		20 nm HKMG	89 mm <sup>2</sup>	2x Typhoon 1.4 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 1 MB L3: 4 MB	PowerVR GX6450 (4C) @ 450 MHz (115.2 GFLOPS)	1GB 64-bit SCh LPDDR3-1600 (12.8 GB/sec)	9/2014	iPhone 6 iPhone 6 Plus
<b>A8X</b>	APL1012		20 nm HKMG	128 mm <sup>2</sup>	3xTyphoon 1.5 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 2 MB L3: 4 MB	PowerVR GX6850 (5C) @ 450 MHz (230.4 GFLOPS)	2 GB 64-bit DCh LPDDR3-1600 (25.6 GB/sec)	10/2014	iPad Air 2
<b>A9</b>	APL1022 (TSMC) APL0898 (Samsung)		16 nm FinFET 14 nm FinFET	104.5 mm <sup>2</sup>	2xTwister 1.85 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: 4 MB	PowerVR GT7600 (6C) @ 450 MHz (172.8 GFLOPS)	2 GB 64-bit SCh LPDDR4-3200 (25.6 GB/sec)	9/2015	iPhone 6s iPhone 6s Plus iPhone SE
<b>A9X</b>	APL1021 (TSMC)		16 nm FinFET	147 mm <sup>2</sup>	2xTwister 2.16-2.26 GHz	ARMv8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB L3: none	PowerVR 7XT series (12C) @ n.a. MHz (345.6 GFLOPS)	2 GB/4 GB 64-bit DCh LPDDR4-3200 (51.2 GB/sec)	11/2015	iPad Pro 9.7" iPad Pro 12.9"

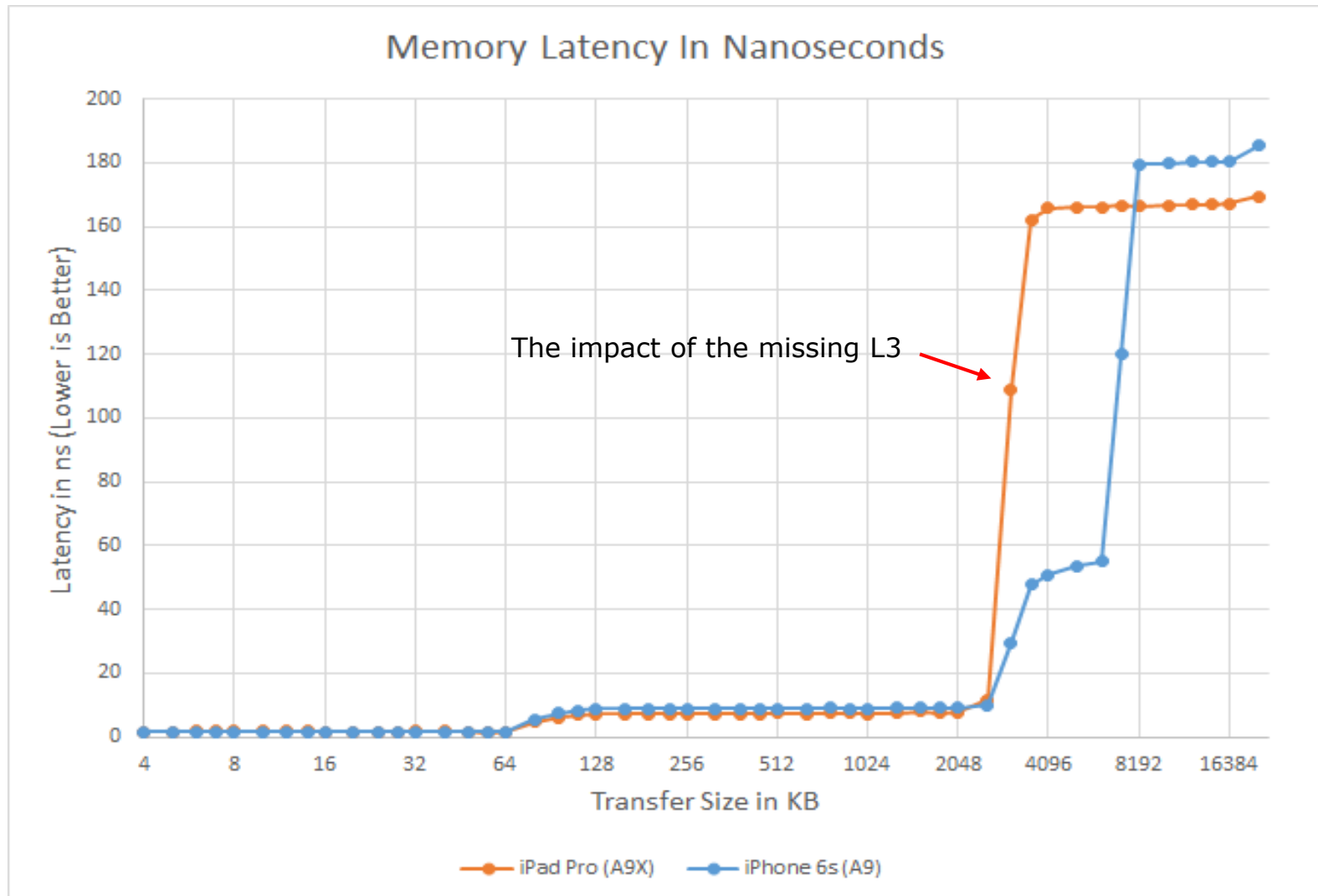
## 9. Apple A9X with dual Twister cores (3)

Die plot of the A9X including 12 graphics cores [43]



## 9. Apple A9X with dual Twister cores (4)

Memory latency (ns) vs. transfer size (KB) of the A9X and A9 memory [41]



## 10. Apple A10 with quad big.LITTLE cores



## 10. Apple A10 with quad big.LITTLE cores (1)

### 10. Apple A10 with quad big.LITTLE cores -1

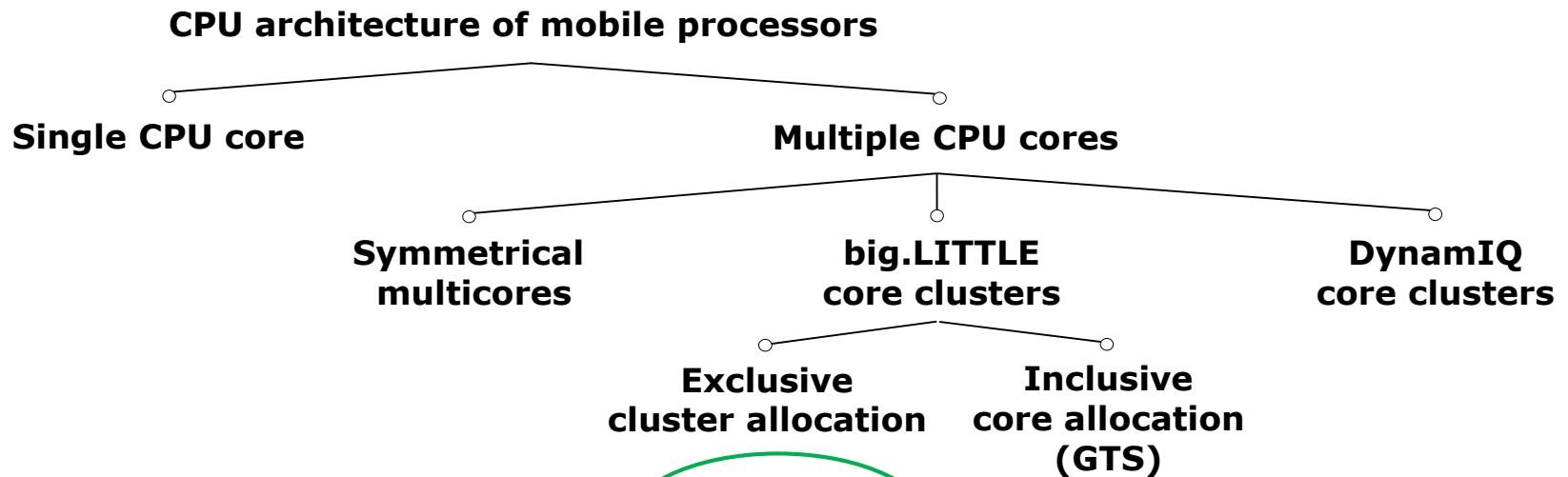
- The A10 was released along with the iPhone 7 and iPhone 7s in 9/2016.
- It includes Apple's first quad core CPU (in big.LITTLE configuration) replacing symmetrical multicores used in prior A-series processors.
  - There are two performance cores, called Hurricane, clocked up to 2.34 GHz
  - and two high efficiency cores, called Zephyr, clocked up to 1.1 GHz (?).

The high performance cores are 40 percent faster than those of the A9 chip and the high-efficiency cores consume only 20 % of the high performance cores.

- The CPU makes use of Apple's first gen. performance controller that allows to utilize simultaneously either the big or the LITTLE cores (called cluster migration).

# 10. Apple A10 with quad big.LITTLE cores (2)

## Apple's A10 position within the evolution of mobile CPU cores



Apple	ARM1176 (2007) until A4 (2010)	→	A5 (2011) (2C)	→	A10 (2016) (2+2)	→	A11 (2017) (2+4)		
Samsung Exynos	3110 (2010)	→	3250 2C (2011) 4412 4C (2012)	→	5410 (2013) (4+4)	→	5420 (2013) (4+4)	→	9810 (2018) (4+4)
Qualcomm Snapdragon	MSM 7225 (2007)	→	8260 2C (2013) 400 4C (2013)	→		→	808 (2+4) (2014) 810 (4+4) (2015)	→	845 (2018) (4+4)
Huawei Kirin	(K3V1) (2009)	→	(K3V2 (2012))	→		→	920 (4+4)) 2014)		
MediaTek	MT6218B (2003)	→	MT6582 4C (2013) MT6592 8C (2013)	→		→	MT6595 8C (2014)		

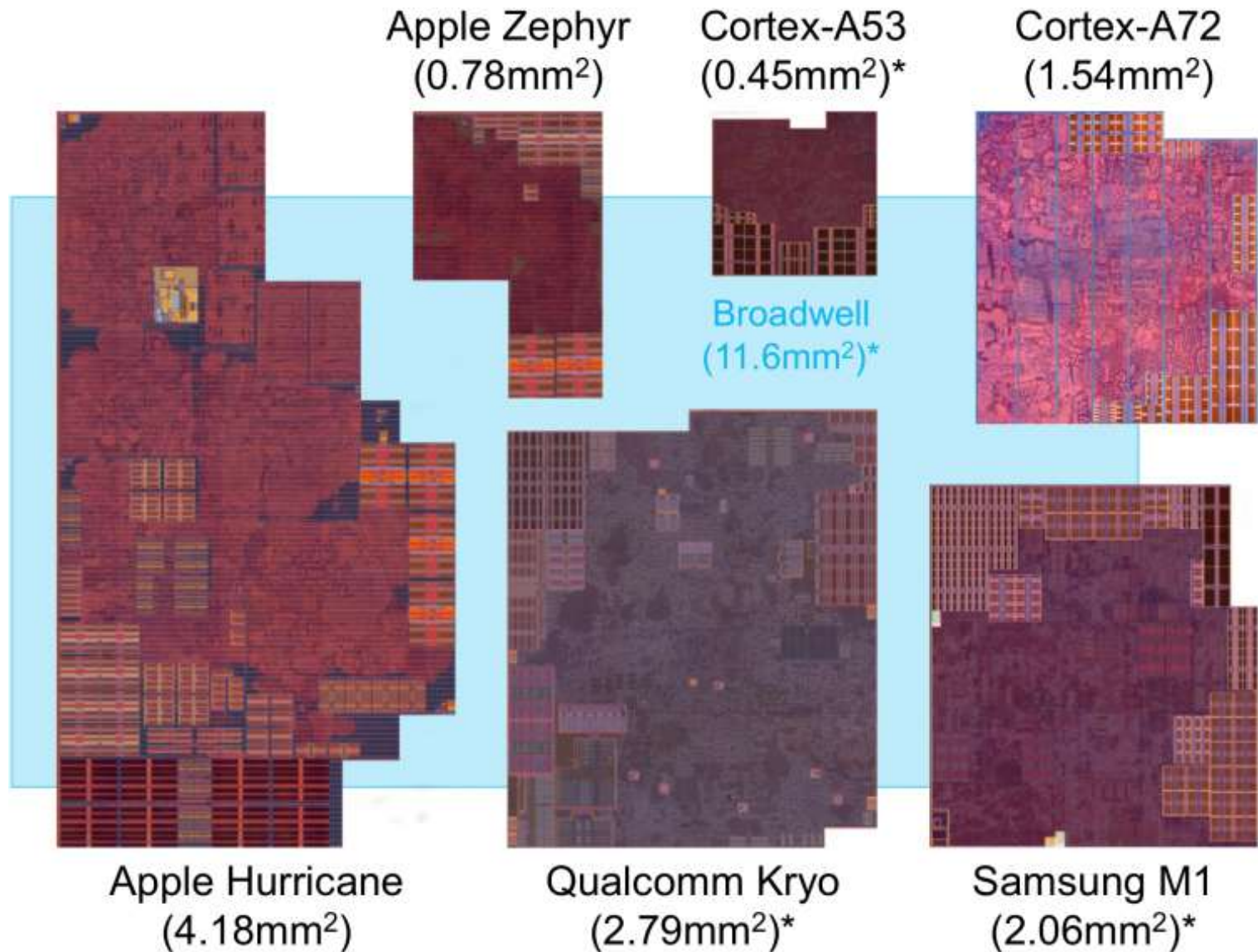
## 10. Apple A10 with quad big.LITTLE cores (3)

### 10. Apple A10 quad big.LITTLE cores -2

- Apple utilizes the **same GPU** as the A9 (Imagination Technology's GT7600) but **parts of the original design were replaced** to achieve 50 % speed-up and 66 % less power consumption vs. the original design.
- The A10 is manufactured by TSMC's **16 nm FinFET** process and includes **3.3 billion transistors on a Si area of 125 mm<sup>2</sup>**.




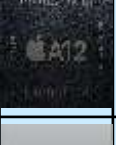

## 10. Apple A10 with quad big.LITTLE cores (4)

Core areas of different mobile processors [50]



# 10. Apple A10 with quad big.LITTLE cores (5)

## Main features of the A10 Fusion SoC

Appl. proc.S	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache (big core)	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A10 (Fusion)</b>	APL1W24		16 nm FinFET	125 mm <sup>2</sup>	2xHurricane (2.34 GHz)+ 2x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 Plus (6C) @ >650 MHz (>250 GFLOPS) (redesigned)	2 GB/3 GB LPDDR4	9/2016	iPhone 7 iPhone 7 Plus
<b>A10X (Fusion)</b>	APL1071 (TSMC)		10 nm FinFET	96.4 mm <sup>2</sup>	3xHurricane (2.38 GHz)+ 3x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: none	PowerVR GT7600 Plus (12C)	3 GB/4 GB LPDDR4	6/2017	iPad Pro 10.5" iPad Pro 12.9" Apple TV 4K
<b>A11 Bionic</b>	APL1W72 (TSMC)		10 nm FinFET	88 mm <sup>2</sup>	2x Monsoon (2.38 GHz) + 4x Mistral (1.69 GHz)z	ARM V8.2-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: 4 MB	Apple Custom GPU (3C)	2 GB/3 GB? LPDDR4X	9/2017	iPhone 8 iPhone 8 Plus iPhone X
<b>A12 Bionic</b>	APL1W82 (TSMC)		7 nm FinFET	83 mm <sup>2</sup>	2x Vortex (2.50 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	3 GB/4 GB LPDDR4X	9/2018	iPhone XS 5.8" iPhone XS Max iPhone XR 6.1"
<b>A12X Bionic</b>	APL1083 (TSMC)		7 nm FinFET	122 mm <sup>2</sup>	4x Vortex (2.48 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (7C)	4 GB/6 GB LPDDR4X	10/2018	iPad Pro 11" iPad Pro 12.9"

LS: System cache, it services the entire SoC

## 10. Apple A10 with quad big.LITTLE cores (6)

Die plot of the A10 as revealed from Chipworks [45]





# 10. Apple A10 with quad big.LITTLE cores (7)

## Main features of Apple's iPhone7 and iPhone7 Plus mobiles [51]

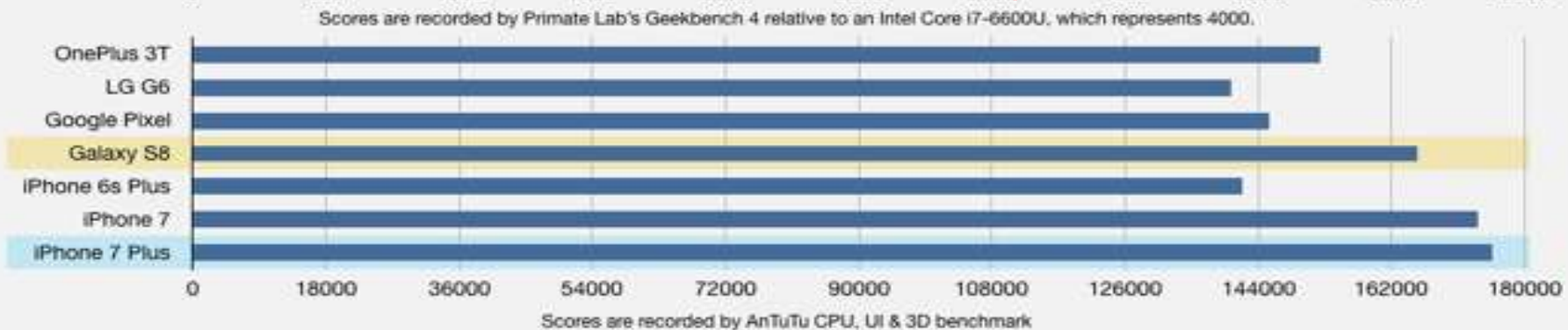
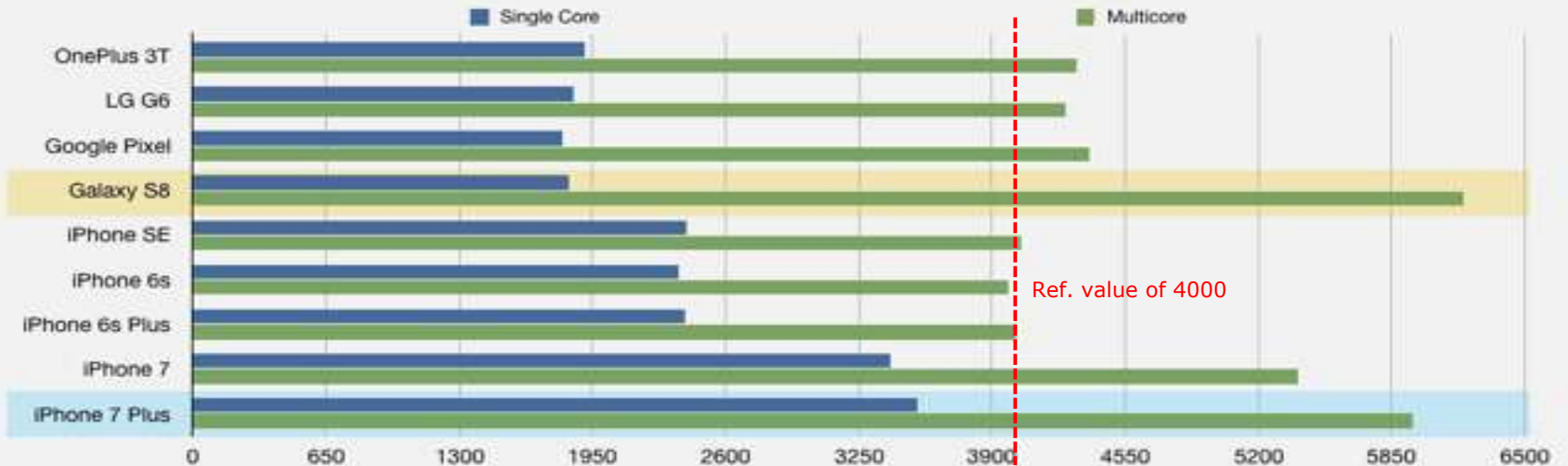
Apple iPhone 7 and 7 Plus				
	Apple iPhone 7	Apple iPhone 7 Plus	Apple iPhone 6s	Apple iPhone 6s Plus
<b>SoC</b>	Apple A10 Fusion 2 x 2.34 GHz Hurricane 2x 1.1 GHz? Zephyr		Apple A9 2 x 1.85GHz Apple Twister	
<b>GPU</b>	6 Core PowerVR Plus GPU		PowerVR GT7600	
<b>Display</b>	4.7-inch 1334 x 750 IPS LCD, DCI-P3	5.5-inch 1920 x 1080 IPS LCD, DCI-P3	4.7-inch 1334 x 750 IPS LCD, sRGB	5.5-inch 1920 x 1080 IPS LCD, sRGB
<b>Size / Mass</b>	138.3 x 67.1 x 7.1 mm, 138 grams	158.2 x 77.9 x 7.3 mm, 188 grams	138.3 x 67.1 x 7.1 mm, 143 grams	158.2 x 77.9 x 7.3mm, 192 grams
<b>Battery</b>	1960 mAh (7.55Whr)	2900 mAh (11.17Whr)	1715 mAh (6.6Whr)	2750 mAh (10.59Whr)
<b>Rear Cameras</b>	12MP <i>f</i> /1.8 OIS, Wide Color Gamut, Quad LED True Tone Flash	12MP <i>f</i> /1.8 wide angle, OIS, Wide Color Gamut, Quad LED True Tone Flash  12MP <i>f</i> /2.8 telephoto, 2x optical zoom, Wide Color Gamut, Quad LED True Tone Flash	12MP with 1.22µm pixels + True Tone Flash	12MP with 1.22µm pixels + True Tone Flash + OIS
<b>Front Camera</b>	7MP <i>f</i> /2.2, Wide Color Gamut, Retina Flash	7MP <i>f</i> /2.2, Wide Color Gamut, Retina Flash	5MP F/2.2 + Retina Flash	5MP F/2.2 + Retina Flash
<b>Storage</b>	32GB/128GB/256GB		16GB/64GB/128GB (Launch) 32GB/128GB (Refresh)	
<b>I/O</b>	Apple Lightning connector		Apple Lightning connector, 3.5mm headset	
<b>WiFi</b>	2.4/5GHz 2x2 802.11a/b/g/n/ac, BT 4.2, NFC		2.4/5GHz 2x2 802.11a/b/g/n/ac, BT 4.2, NFC	
<b>Launch Price</b>	\$649/749/849 32/128/256GB	\$769/869/969 32/128/256GB	\$649/749/849 16/64/128GB	\$749/849/949 16GB/64/128GB



# 10. Apple A10 with quad big.LITTLE cores (8)

Geekbench 4 and AnTuTu benchmark results of high-end mobiles [52]

Geekbench 4	OnePlus 3T	LG G6	Google Pixel	Galaxy S8	iPhone SE	iPhone 6s	iPhone 6s Plus	iPhone 7	iPhone 7 Plus
Single Core	1912	1856	1806	1838	2410	2374	2399	3406	3538
Multicore	4314	4261	4377	6202	4043	3982	4019	5394	5953
AnTuTu 3D	152376	140374	145469	165521	no score	no score	141813	173642	175606
Processor	Qualcomm SD 821 (Adreno 530)			SD 835/A540	A9	A9	A9	A10 Fusion	A10 Fusion
Peak CPU	2.35 GHz	2.35 GHz	2.15 GHz	2.35 GHz	1.8 GHz	1.85 GHz	1.85 GHz	2.34 GHz	2.34 GHz
RAM	6 GB	4 GB	4 GB	4 GB	1 GB	2 GB	2 GB	2 GB	3 GB



## 10. Apple A10 with quad big.LITTLE cores (9)

**Remark:** Geekbench 4 benchmarks are measured using a Microsoft Surface Book with an Intel Core i7-6600U (Skylake) processor as a baseline with a score of 4000 points [62].

Main features of the reference system:

- # of Cores: 2
- # of Threads: 4
- Processor Base Frequency: 2.60 GHz
- Max Turbo Frequency: 3.40 GHz
- Cache: 4 MB
- TDP: 15 W
- Graphics: Intel HD Graphics 520

## 11. Apple A10X with hexa big.LITTLE cores




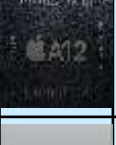

## 11. Apple A10X with hexa big.LITTLE cores (1)

### 11. Apple A10X with hexa big.LITTLE cores

- Introduced in 6/2017.
- Fabricated on TSMCs 10nm FinFET process on 96 mm<sup>2</sup> Si area.
- It includes
  - 3 Hurricane and 3 Zephyr cores instead of 2+2 cores as the A10 does and
  - 3 to 4 GB LPDDR4 RAM rather than 2 to 3 GB as the A10.
- It appeared in the 10.5" iPad Pro and 12.9" iPad Pro tablet models, called also as the 2. generation iPad Pro models.

# 11. Apple A10X with hexa big.LITTLE cores (2)

## Main features of the A10X Fusion SoC

Appl. proc.S	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache (big core)	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A10 (Fusion)</b>	APL1W24		16 nm FinFET	125 mm <sup>2</sup>	2xHurricane (2.34 GHz)+ 2x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 Plus (6C) @ >650 MHz (>250 GFLOPS) (redesigned)	2 GB/3 GB LPDDR4	9/2016	iPhone 7 iPhone 7 Plus
<b>A10X (Fusion)</b>	APL1071 (TSMC)		10 nm FinFET	96.4 mm <sup>2</sup>	3xHurricane (2.38 GHz)+ 3x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: none	PowerVR GT7600 Plus (12C)	3 GB/4 GB LPDDR4	6/2017	iPad Pro 10.5" iPad Pro 12.9" Apple TV 4K
<b>A11 Bionic</b>	APL1W72 (TSMC)		10 nm FinFET	88 mm <sup>2</sup>	2x Monsoon (2.38 GHz) + 4x Mistral (1.69 GHz)	ARM V8.2-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: 4 MB	Apple Custom GPU (3C)	2 GB/3 GB? LPDDR4X	9/2017	iPhone 8 iPhone 8 Plus iPhone X
<b>A12 Bionic</b>	APL1W82 (TSMC)		7 nm FinFET	83 mm <sup>2</sup>	2x Vortex (2.50 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	3 GB/4 GB LPDDR4X	9/2018	iPhone XS 5.8" iPhone XS Max iPhone XR 6.1"
<b>A12X Bionic</b>	APL1083 (TSMC)		7 nm FinFET	122 mm <sup>2</sup>	4x Vortex (2.48 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (7C)	4 GB/6 GB LPDDR4X	10/2018	iPad Pro 11" iPad Pro 12.9"

LS: System cache, it services the entire SoC

**Note** that the A10X Fusion SoC has

- 3 Hurricane and 3 Zephyr cores rather than only 2+2 cores as the A10 SoC and
- 3 to 4 GB LPDDR4 RAM rather than 2 to 3 GB as the A10 SoC.

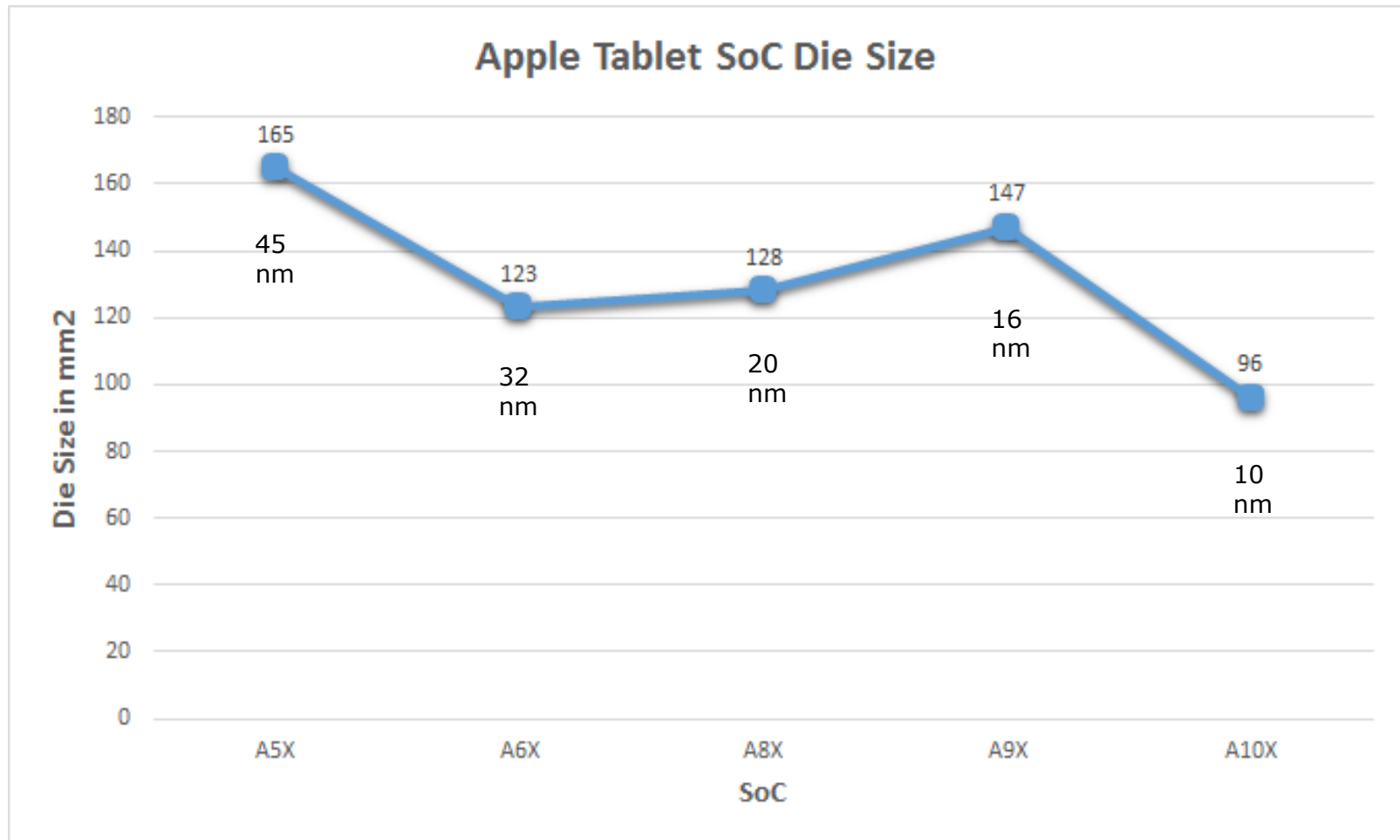
## 11. Apple A10X with hexa big.LITTLE cores (3)

### Main features of Apple's A6X to A10X tablet SoCs [49]

Apple SoC Comparison				
	A10X	A9X	A8X	A6X
<b>CPU</b>	3x Hurricane + 3x Zephyr	2x Twister	3x Typhoon	2x Swift
<b>CPU Clockspeed</b>	~2.36GHz	2.26GHz	1.5GHz	1.3GHz
<b>GPU</b>	12 Cluster GPU	PVR 12 Cluster Series7	Apple/PVR GXA6850	PVR SGX554 MP4
<b>Typical RAM</b>	4GB LPDDR4	4GB LPDDR4	2GB LPDDR3	1GB LPDDR2
<b>Memory Bus Width</b>	128-bit	128-bit	128-bit	128-bit
<b>Memory Bandwidth</b>	TBD	51.2GB/sec	25.6GB/sec	17.1GB/sec
<b>L2 Cache</b>	8MB	3MB	2MB	1MB
<b>L3 Cache</b>	None	None	4MB	N/A
<b>Manufacturing Process</b>	TSMC 10nm FinFET	TSMC 16nm FinFET	TSMC 20nm	Samsung 32nm

## 11. Apple A10X with hexa big.LITTLE cores (4)

Die size of Apple's A5X to A10X tablet SoCs [49]





# 11. Apple A10X with hexa big.LITTLE cores (5)

## Main features of Apple's A9X and A10X based tablets [60]

	iPad Pro 10.5" (2017)	iPad Pro 12.9" (2017)	iPad Pro 9.7" (2016)	iPad Pro 12.9" (2015)
<b>SoC</b>	Apple A10X Fusion 3x Apple Hurricane performance cores 3x Apple Zephyr efficiency cores		Apple A9X 2x Apple Twister @ ~2.2GHz	
	12 core GPU		PowerVR 12 Cluster Series7XT	
<b>Display</b>	10.5-inch 2224x1668 IPS LCD DCI-P3, 120Hz	12.9-inch 2732x2048 IPS LCD DCI-P3, 120Hz	9.7-inch 2048x1536 IPS LCD DCI-P3	12.9-inch 2732x2048 IPS LCD sRGB
<b>Dimensions</b>	250.6 x 174.1 x 6.1 mm 469 / 477 grams (WiFi / LTE)	305.7 x 220.6 x 6.9 mm 677 / 692 grams (WiFi / LTE)	240.0 x 169.5 x 6.1 mm 437 / 444 grams (WiFi / LTE)	305.7 x 220.6 x 6.9 mm 713 / 723 grams (WiFi / LTE)
<b>RAM</b>	?	4GB LPDDR4	2GB LPDDR4	4GB LPDDR4
<b>NAND</b>	All: 64GB / 256GB / 512 GB		All: 32GB / 128GB / 256GB	WiFi: 32GB / 128GB / 256GB WiFi + Cellular: 128GB / 256GB
<b>Battery</b>	30.4 Wh	41.0 Wh	27.5 Wh	38.5 Wh
<b>Front Camera</b>	7MP, f/2.2, Auto HDR, Wide Color Gamut, Retina Flash		5MP, f/2.2	1.2MP, f/2.2
<b>Rear Camera</b>	12MP, 1.22µm pixels, f/1.8, PDAF, OIS, Auto HDR, Wide Color Gamut, True Tone Quad-LED flash		12MP, 1.22µm pixels, f/2.2, True Tone LED flash	8MP, 1.1µm pixels, f/2.4
<b>Cellular</b>	2G / 3G / 4G LTE (Category 9)		2G / 3G / 4G LTE (Category 4)	
<b>SIM Size</b>	NanoSIM		NanoSIM	
<b>Wireless</b>	802.11a/b/g/n/ac 2x2 MIMO, BT 4.2 LE, GPS/GLONASS		802.11a/b/g/n/ac 2x2 MIMO, BT 4.2 LE, GPS/GLONASS	
<b>Connectivity</b>	Wi-Fi/Wi-Fi+LTE		Wi-Fi	
<b>Launch OS</b>	iOS 10		iOS 9	
<b>Launch Price</b>	649-1229 \$		599-1079 \$	

## 12. Apple A11 with dual big and quad LITTLE cores



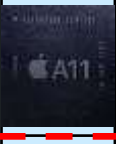


## 12. Apple A11 with dual big and quad LITTLE cores (1)

### 12. Apple A11 with dual big and quad LITTLE cores

- Introduced in [9/2017](#) along with the [iPhone 8](#), [iPhone 8 Pro](#) and [iPhone X](#).
- It is Apple's **first 10 nm** SoC, manufactured by TSMC as a PoP package with 2GB LPDDR4X memory in the iPhone 8 and 3 GB LPDDR4 memory in the iPhone 8 Plus and iPhone X.
- It is based on the [ARMv8.2-A ISA](#) (supporting therefore e.g. FP16 processing).
- Transistor count: [4.3 billion](#).

## 12. Apple A11 with dual big and quad LITTLE cores (2)

### Main features of the A11 Bionic SoC

Appl. proc.S69696	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache (big core)	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A10 (Fusion)</b>	APL1W24		16 nm FinFET	125 mm <sup>2</sup>	2xHurricane (2.34 GHz)+ 2x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 Plus (6C) @ >650 MHz (>250 GFLOPS) (redesigned)	2 GB/3 GB LPDDR4	9/2016	iPhone 7 iPhone 7 Plus
<b>A10X (Fusion)</b>	APL1071 (TSMC)		10 nm FinFET	96.4 mm <sup>2</sup>	3xHurricane (2.38 GHz)+ 3x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: none	PowerVR GT7600 Plus (12C)	3 GB/4 GB LPDDR4	6/2017	iPad Pro 10.5" iPad Pro 12.9" Apple TV 4K
<b>A11 Bionic</b>	APL1W72 (TSMC)		10 nm FinFET	88 mm <sup>2</sup>	2x Monsoon (2.38 GHz) + 4x Mistral (1.69 GHz)	ARM V8.2-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: 4 MB	Apple Custom GPU (3C)	2 GB/3 GB? LPDDR4X	9/2017	iPhone 8 iPhone 8 Plus iPhone X
<b>A12 Bionic</b>	APL1W82 (TSMC)		7 nm FinFET	83 mm <sup>2</sup>	2x Vortex (2.50 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	3 GB/4 GB LPDDR4X	9/2018	iPhone XS 5.8" iPhone XS Max iPhone XR 6.1"
<b>A12X Bionic</b>	APL1083 (TSMC)		7 nm FinFET	122 mm <sup>2</sup>	4x Vortex (2.48 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (7C)	4 GB/6 GB LPDDR4X	10/2018	iPad Pro 11" iPad Pro 12.9"

LS: System cache, it services the entire SoC

## 12. Apple A11 with dual big and quad LITTLE cores (3)

### Main features of the Apple A11 Bionic SoC [53]

Model	Apple iPhone7	Apple iPhone8 256 GB	Apple iPhone8 Plus	Apple iPhone X
Launched	10/2016	09/2017	09/2017	11/2017
SoC	Apple A10 Fusion APL1024	Apple A11 Bionic		
CPU	DC Hurricane (2.34 GHz) + DC Zephyr (1.1 GHz)	DC Monsoon (2.39 GHz) + QC Mistral (1.42 GHz)		
GPU	PowerVR GT7600 Plus	In-house 3 cores		
NPU	--	Dual core		
ISP	Yes	In-house		
Coprocessor	M10 motion	M11 Motion		
RAM	2 GB	2 GB	3 GB	3 GB
Flash memory	32 GB	256 GB	64 /256 GB	64/256 GB
Technology	16 nm	10 nm		

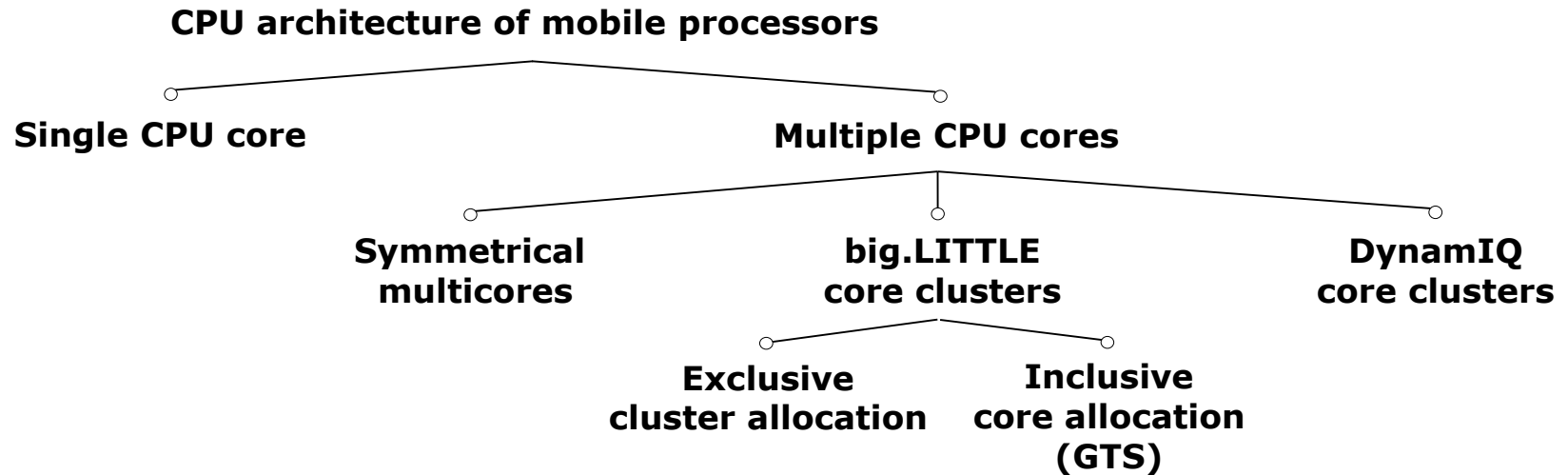
## 12. Apple A11 with dual big and quad LITTLE cores (4)

### 12. A11 Bionic

- The A11 Bionic SoC has
  - two performance cores called **Monsoon**, clocked at 3.39 GHz and
  - four high efficiency cores, called **Mistral**, clocked at 1.42 GHz.
- The performance cores are 25 percent faster than those of the A10 chip, and the high-efficiency cores are 70 percent faster those of the A10 chip.
- It makes use of a new, **2. gen. performance controller** that allows to utilize **up to all six cores simultaneously**, if needed (in contrast to the prior controller that activated either the big or the LITTLE cores).

## 12. Apple A11 with dual big and quad LITTLE cores (5)

### Apple's A11 position within the evolution of mobile CPU cores



Apple	ARM1176 (2007) until A4 (2010)	→	A5 (2011) (2C)	→	A10 (2016) (2+2)	→	A11 (2017) (2+4)		
Samsung Exynos	3110 (2010)	→	3250 2C (2011) 4412 4C (2012)	→	5410 (2013) (4+4)	→	5420 (2013) (4+4)	→	9810 (2018) (4+4)
Qualcomm Snapdragon	MSM 7225 (2007)	→	8260 2C (2013) 400 4C (2013)	→		→	808 (2+4) (2014) 810 (4+4) (2015)	→	845 (2018) (4+4)
Huawei Kirin	(K3V1) (2009)	→	(K3V2 (2012))	→		→	920 (4+4)) 2014)		
MediaTek	MT6218B (2003)	→	MT6582 4C (2013) MT6592 8C (2013)	→		→	MT6595 8C (2014)		

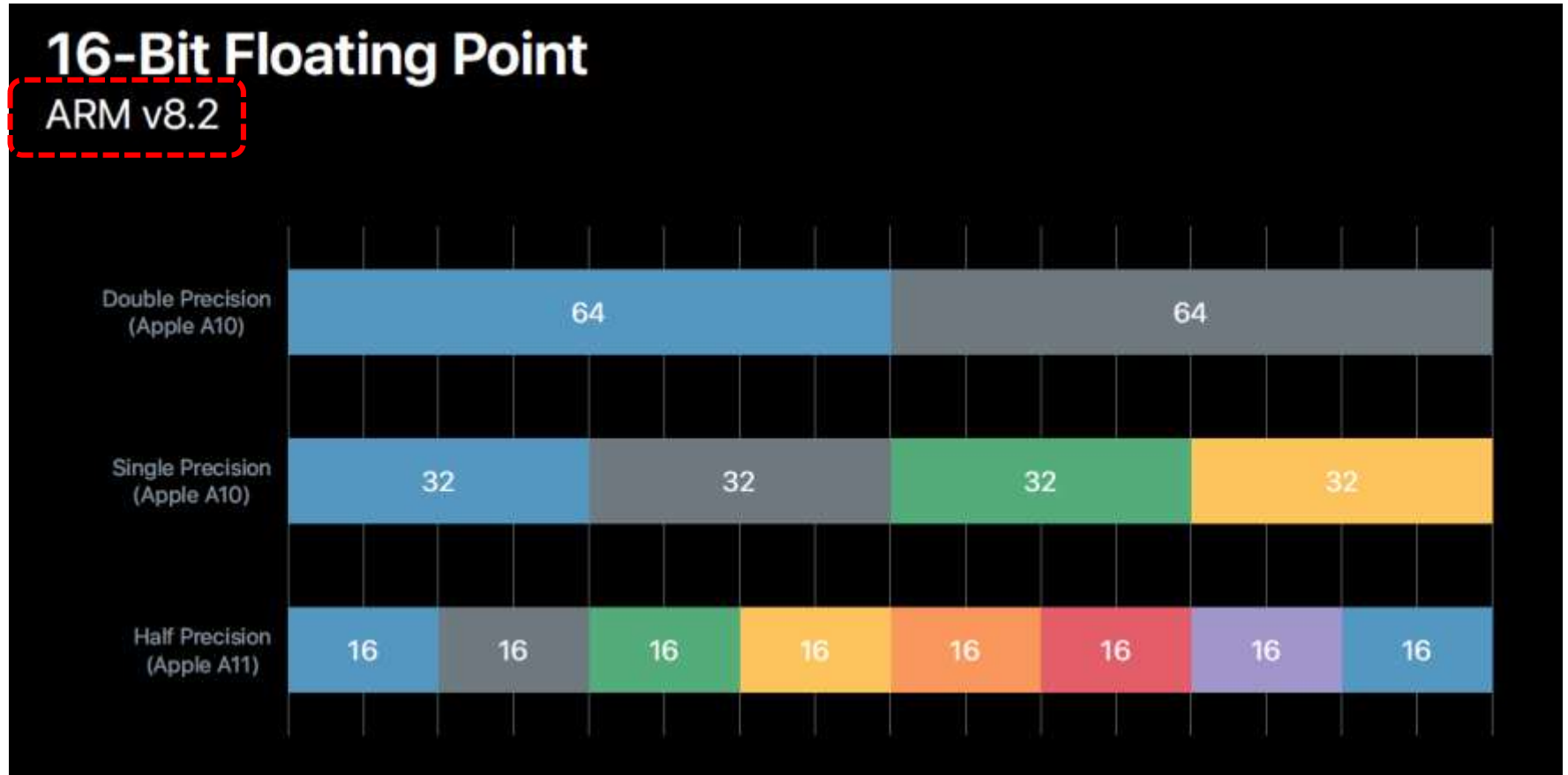


## 12. Apple A11 with dual big and quad LITTLE cores (6)

### 12. A11 Bionic -2

- It is Apple's first SoC with an **in-house designed GPU (including 3 cores)** that has about the same performance as the prior PowerVR GT7600 from Imagination Technologies, used in the A10 but has 50 % less power consumption.
- It is also Apple's first SoC with a **Neural Engine Unit (NPU)** in order to give higher level support for **AI applications**.
- The A11 Bionic includes **4.3 billion transistors**, much more than Qualcomm's Snapdragon (3 billion) or Intel's desktop quad-core Skylake chip (1.75 billion) [54], on a Si area of **88 mm<sup>2</sup>** (that is 30 % less than that of the A10).

## Support of FP16 [63]



## 12. Apple A11 with dual big and quad LITTLE cores (7)

### A11 Bionic floor plane [55]



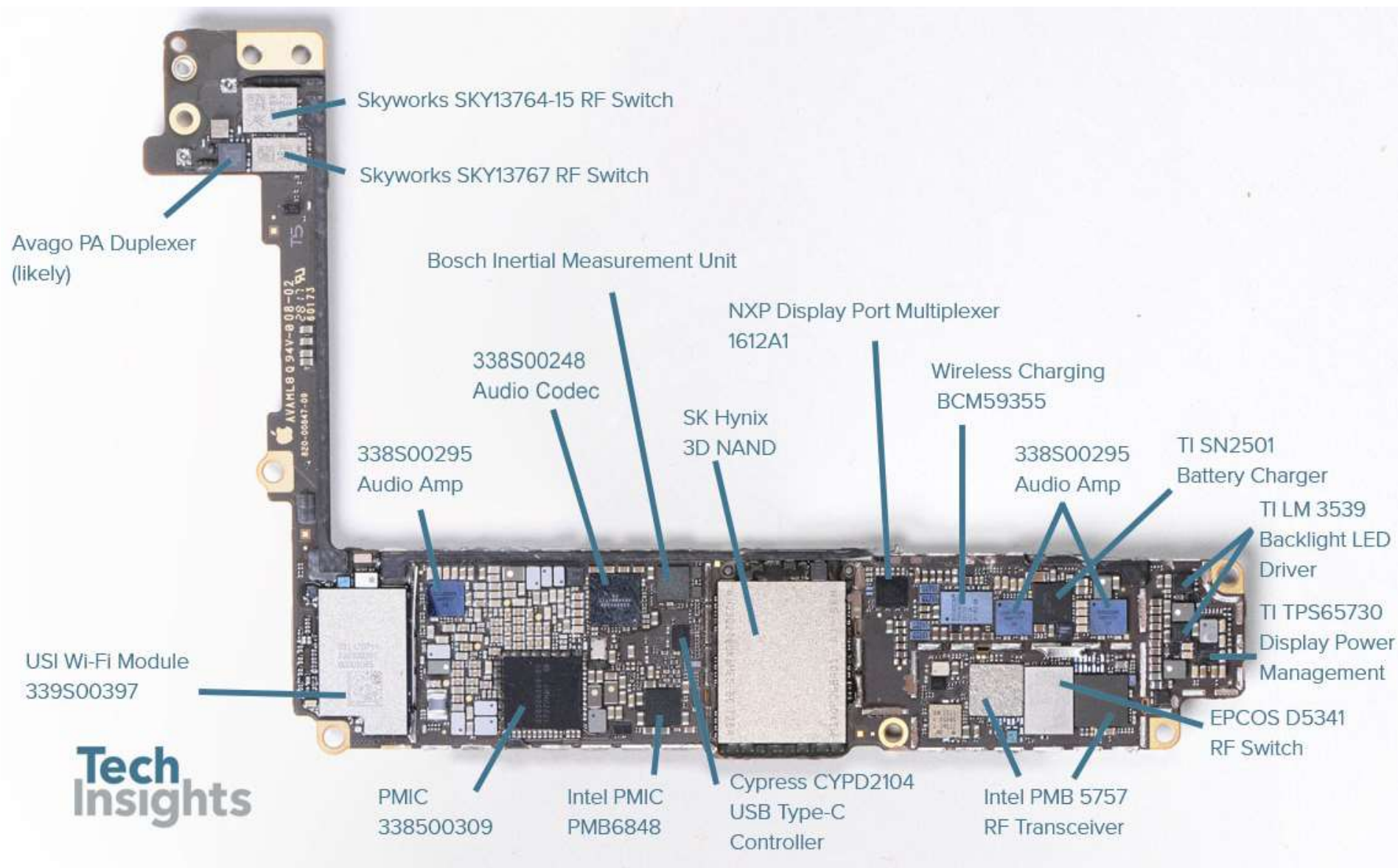
## 12. Apple A11 with dual big and quad LITTLE cores (8)

### The Neural Processing Unit (NPU) [56]

- It is a dedicated **two core hardware unit** to speed up machine learning tasks, including face identification, image enhancements etc.
- The NPU is capable to perform **600 billion operations per second**.
- The NPU allows to perform **AI applications faster and more energy-efficient** than while using the CPU with GPU support.

## 12. Apple A11 with dual big and quad LITTLE cores (9)

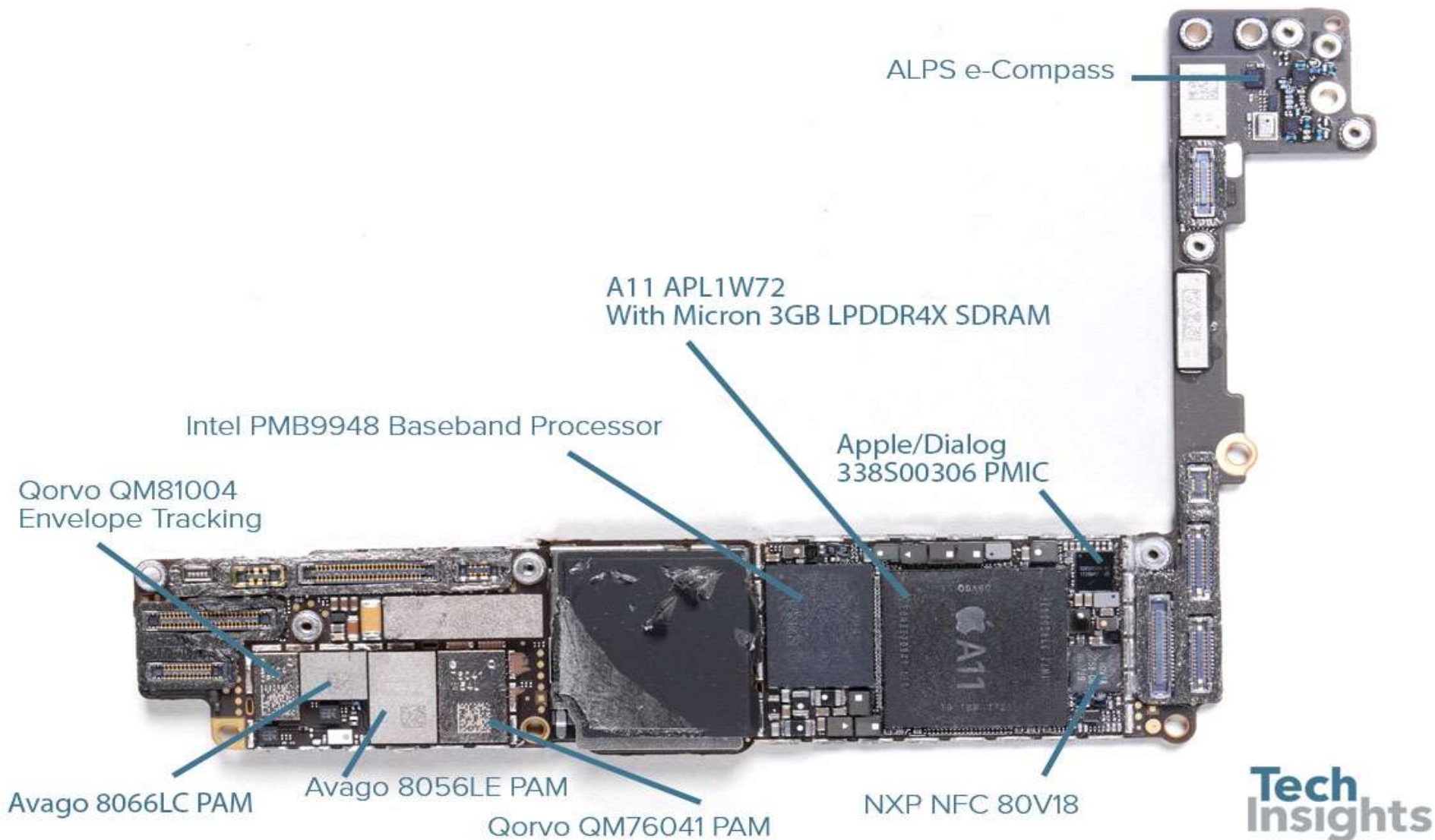
Main components as seen on the motherboard of the iPhone 8 -1 [55]





## 12. Apple A11 with dual big and quad LITTLE cores (10)

Main components as seen on the motherboard of the iPhone 8 -2 [55]



## 12. Apple A11 with dual big and quad LITTLE cores (11)

Apple's Metal 2 graphics API introduced along with the iOS11 and A11 [57]

- Metal is a low-level graphics computing framework that has a number of successive releases with more and more enhancements targeting subsequent iOS and MacOS releases.
- From these releases Apple renamed the one introduced [along with the iOS11 and the A11 Bionic processor](#) as **Metal 2** in 06/2017.
- Metal 2 targets first of all VR and deep learning.

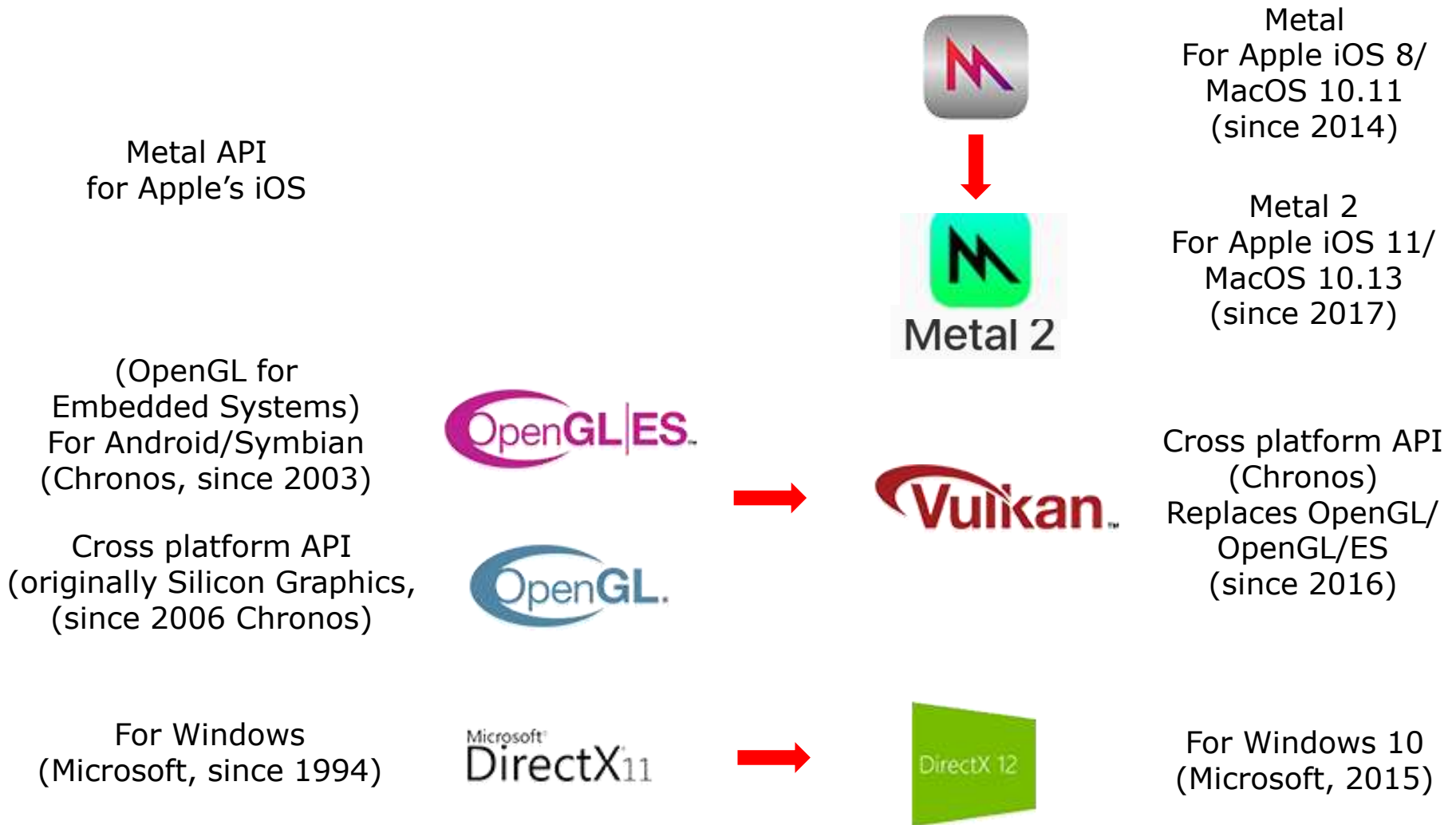
### Remark

Metal 2 introduces among others a [new memory model](#) that adopts and extends the C++11 memory consistency model and atomic functions for [thread synchronization](#) between threads within or across thread groups.



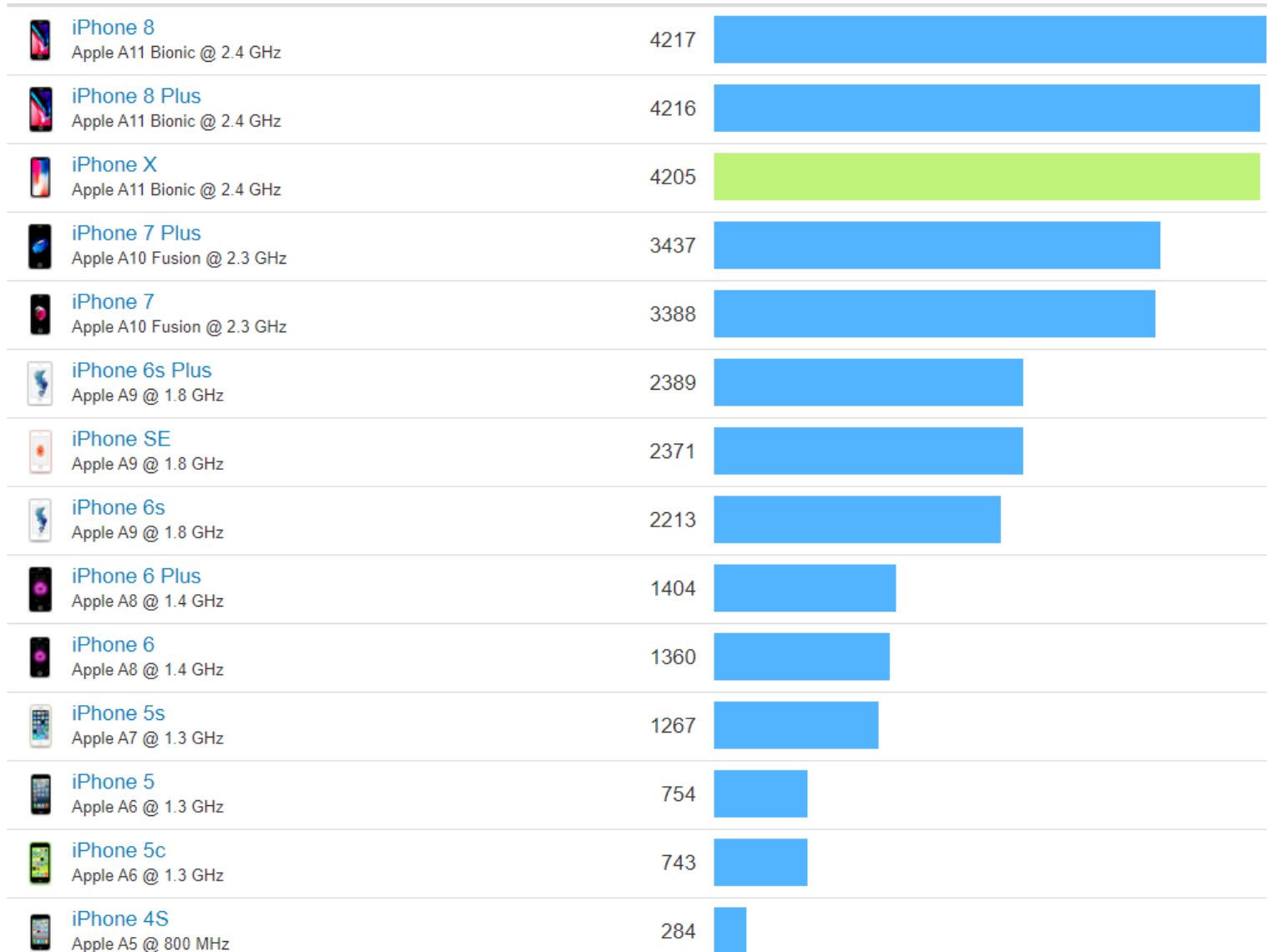
## 12. Apple A11 with dual big and quad LITTLE cores (12)

**Remark:** Low-level graphics and compute APIs



## 12. Apple A11 with dual big and quad LITTLE cores (13)

### Single core Geekbench 4 scores of Apple's iPhones [58]



## 12. Apple A11 with dual big and quad LITTLE cores (14)

Geekbench 4 single core and multi core scores of high-end mobiles [59]

Geekbench 4	MacBook Pro 13" 2017	Huawei P10	Xiaomi Mi 6	Samsung Galaxy S8	iPhone SE	iPhone 7	iPhone 7 Plus	iPhone 8	iPhone 8 Plus	iPhone X
Single Core	4229	1886	1900	1965	2410	3328	3332	4189	4142	4017
Multicore	8959	5763	5996	6495	4043	5545	5558	9983	9883	9286
Processor	Intel Core i5 7267U	Hisilicon Kirin 960	Qualcomm Snapd. 835	Samsung Exynos 8895	A9	A10 Fusion	A10 Fusion	A11 Bionic	A11 Bionic	A11 Bionic
CPU clock	3.5 GHz	2.25 GHz	1.9 GHz	1.6 GHz	1.8 GHz	2.34 GHz	2.34 GHz	?	?	?
RAM	8 GB	4 GB	6 GB	4 GB	1 GB	2 GB	3 GB	2 GB	3 GB	3 GB
Display	2560x1600	1080x1920	1080x1920	1440x2960	640x1136	750x1334	1080x1920	750x1334	1080x1920	1125x2436



Scores are recorded by Primate Lab's Geekbench 4 relative to an Intel Core i7-6600U, which represents 4000.

## 12. Apple A11 with dual big and quad LITTLE cores (15)

**Remark:** Geekbench 4 benchmarks are measured using a Microsoft Surface Book with an Intel Core i7-6600U (Skylake) processor (9/2015) as a baseline with a score of 4000 points [62].

Main features of the reference system:

- # of Cores: 2
- # of Threads: 4
- Processor Base Frequency: 2.60 GHz
- Max Turbo Frequency: 3.40 GHz
- Cache: 4 MB
- TDP: 15 W
- Graphics: Intel HD Graphics 520

13. Apple A12 with dual big and quad LITTLE cores

## 13. Apple A12 with dual big and quad LITTLE cores (1)

### 13. Apple A12 with dual big and quad LITTLE cores






- Introduced in 9/2017 along with the iPhone 8, iPhone 8 Pro and iPhone X.
- It is the first 7 nm commercial SoC, manufactured by TSMC as a PoP package with 4GB LPDDR4x memory in the iPhone XS and XS Max as well as 3 GB LPDDR4x memory in the iPhone XR.
- The A12 incorporates dual Vortex cores (2.50 GHz) and quad Tempest cores (1.59 GHz).

All six cores may run in parallel operated by the 2. gen. Power Controller, introduced along with the A11.

- It executes the ARMv8.3-A ISA.
- Transistor count: 6.9 billion.

# 13. Apple A12 with dual big and quad LITTLE cores (2)

## Main features of the A12 Bionic SoC

Appl. proc.S6	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache (big core)	GPU	Memory (up to)	Intro.	Utilizing devices
<b>A10 (Fusion)</b>	APL1W24		16 nm FinFET	125 mm <sup>2</sup>	2xHurricane (2.34 GHz)+ 2x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 Plus (6C) @ >650 MHz (>250 GFLOPS) (redesigned)	2 GB/3 GB LPDDR4	9/2016	iPhone 7 iPhone 7 Plus
<b>A10X (Fusion)</b>	APL1071 (TSMC)		10 nm FinFET	96.4 mm <sup>2</sup>	3xHurricane (2.38 GHz)+ 3x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: none	PowerVR GT7600 Plus (12C)	3 GB/4 GB LPDDR4	6/2017	iPad Pro 10.5" iPad Pro 12.9" Apple TV 4K
<b>A11 Bionic</b>	APL1W72 (TSMC)		10 nm FinFET	88 mm <sup>2</sup>	2x Monsoon (2.38 GHz) + 4x Mistral (1.69 GHz)	ARM V8.2-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: 4 MB	Apple Custom GPU (3C)	2 GB/3 GB? LPDDR4X	9/2017	iPhone 8 iPhone 8 Plus iPhone X
<b>A12 Bionic</b>	APL1W82 (TSMC)		7 nm FinFET	83 mm <sup>2</sup>	2x Vortex (2.50 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	4 GB/3 GB LPDDR4X	9/2018	iPhone XS 5.8" iPhone XS Max iPhone XR 6.1"
<b>A12X Bionic</b>	APL1083 (TSMC)		7 nm FinFET	122 mm <sup>2</sup>	4x Vortex (2.48 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (7C)	4 GB/6 GB LPDDR4X	10/2018	iPad Pro 11" iPad Pro 12.9"

LS: System cache, it services the entire SoC



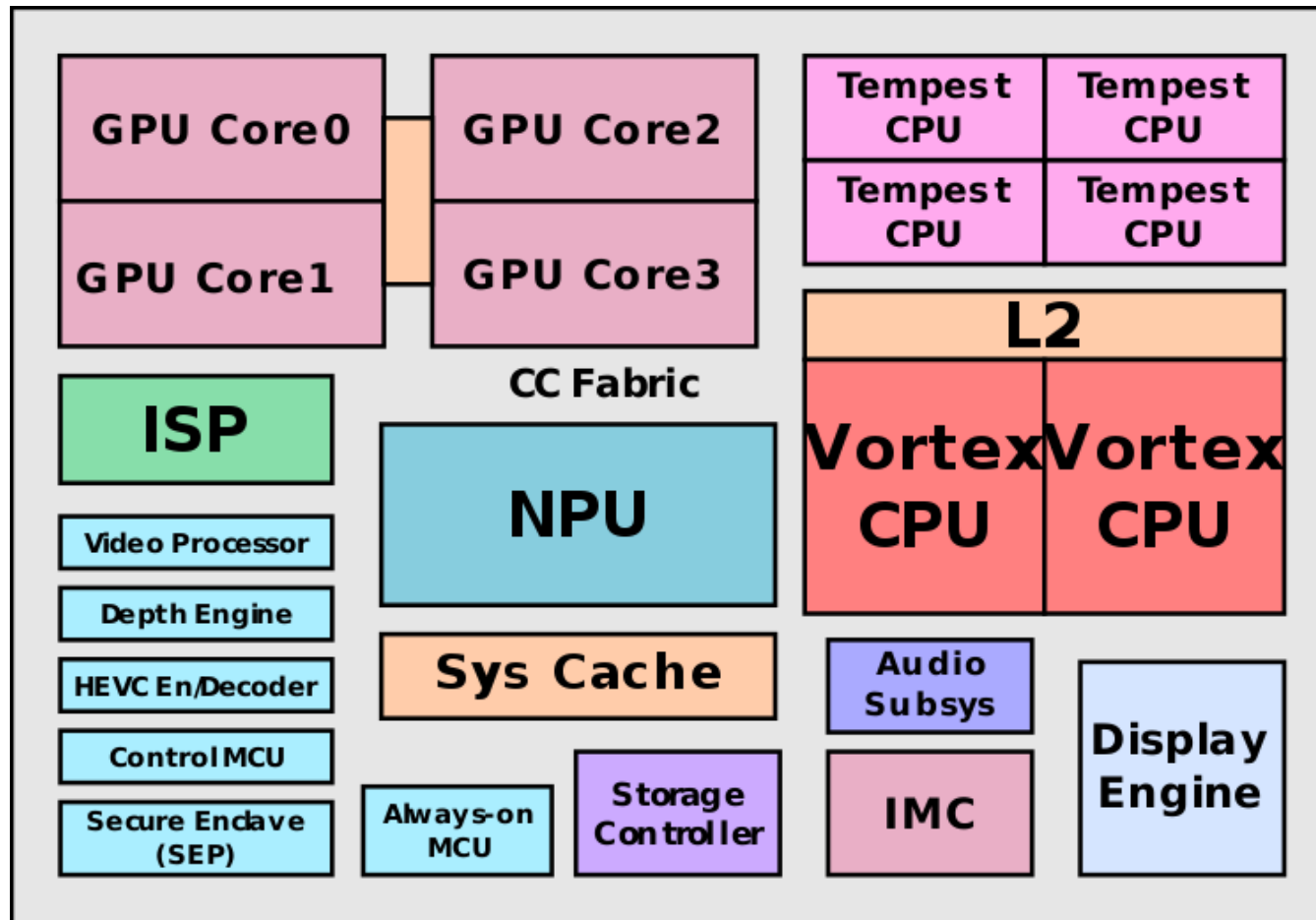
# 13. Apple A12 with dual big and quad LITTLE cores (3)

Max. clock frequency vs. core loading of the A12 [64]

Maximum Frequency vs Loaded Threads Per-Core Maximum MHz						
Apple A11	1	2	3	4	5	6
Big 1	2380	2325	2083	2083	2083	2083
Big 2		2325	2083	2083	2083	2083
Little 1			1694	1587	1587	1587
Little 2				1587	1587	1587
Little 3					1587	1587
Little 4						1587
Apple A12	1	2	3	4	5	6
Big 1	2500	2380	2380	2380	2380	2380
Big 2		2380	2380	2380	2380	2380
Little 1			1587	1562	1562	1538
Little 2				1562	1562	1538
Little 3					1562	1538
Little 4						1538

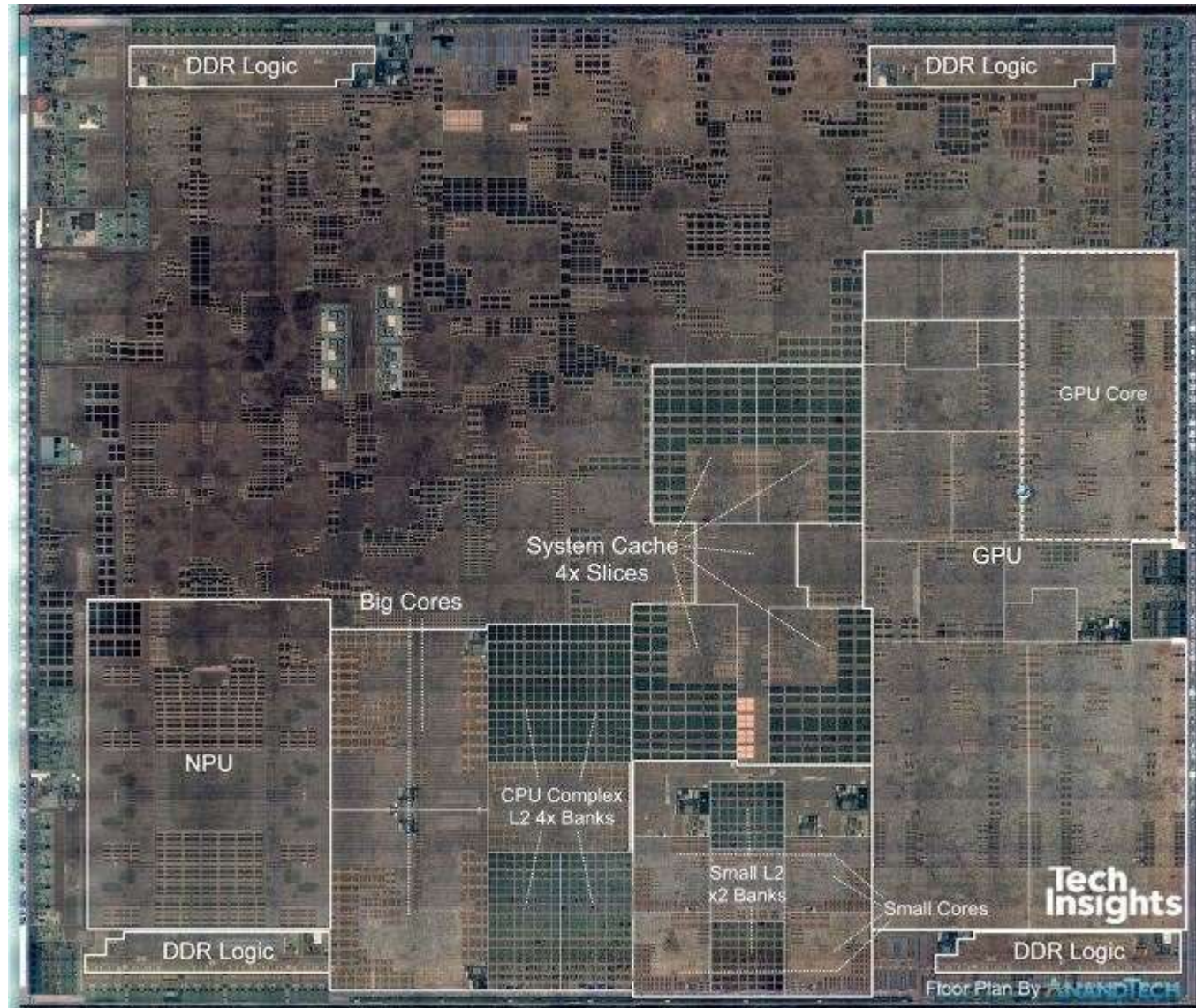
## 13. Apple A12 with dual big and quad LITTLE cores (4)

Main functional units of the A12 Bionic SoC [65]



## 13. Apple A12 with dual big and quad LITTLE cores (5)

### Floor plan of the A12 Bionic SoC [64]



## 13. Apple A12 with dual big and quad LITTLE cores (6)

### Major enhancements

- a) Enhanced cache architecture
- b) Improved neural engine
- c) Improved GPU

## 13. Apple A12 with dual big and quad LITTLE cores (7)

### a) Enhanced cache architecture

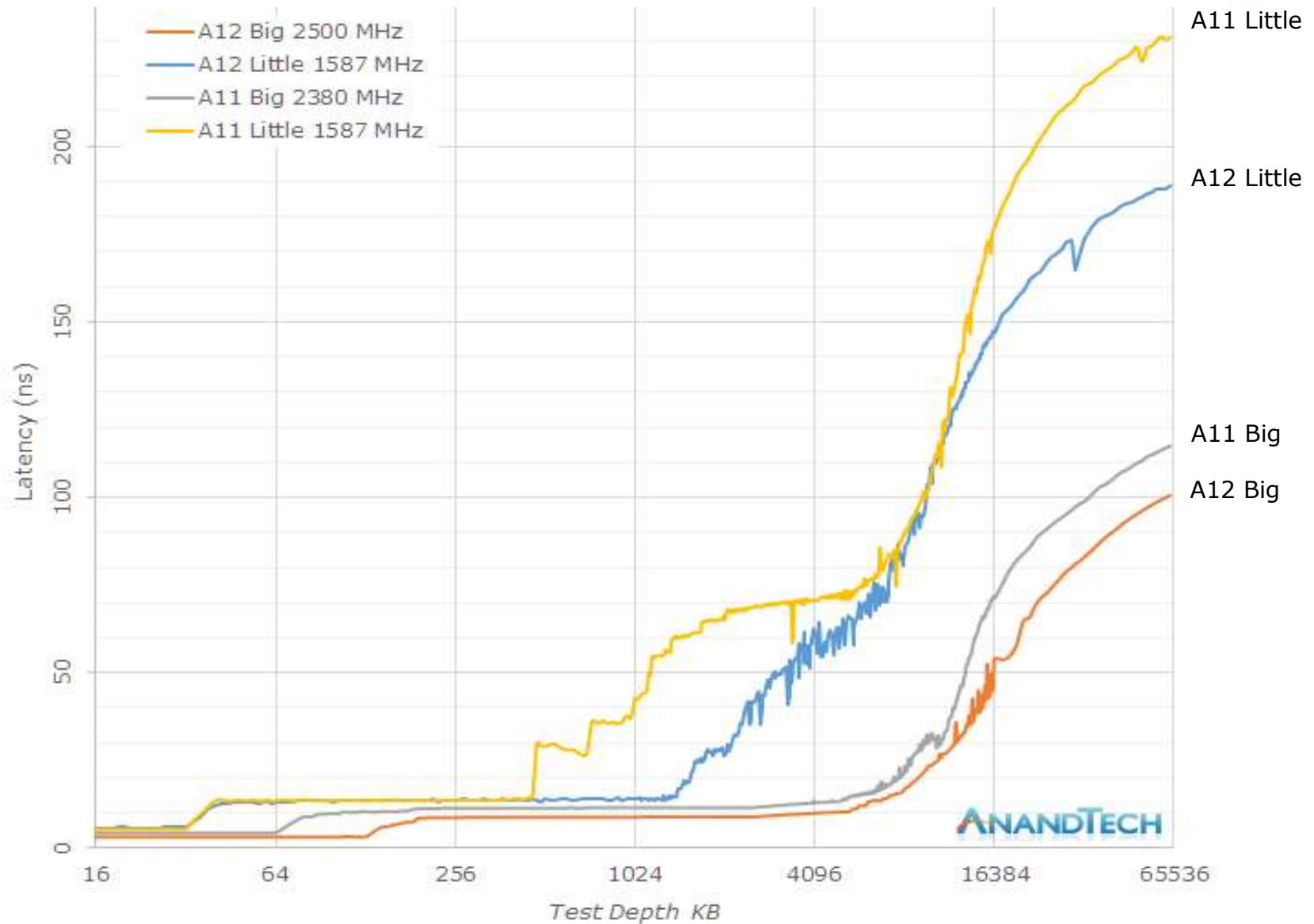
Cache sizes of the A12 vs. the preceding A11 [64]

Measured and Estimated Cache Sizes		
SoC	Apple A12	Apple A11
Big L1\$	128KB	64KB
Big L2\$	128 instances <b>6MB</b> per core/thread <b>8MB total</b> at 64KB/inst	128 instances <b>6MB</b> per core/thread <b>8MB total</b> at 64KB/inst
Small L1\$	32KB	32KB
Small L2\$	32 instances <b>1.5MB</b> per core/thread <b>2MB total</b> at 64KB/inst	16 + 2(?) instances <b>512KB</b> per core/thread <b>1MB total</b> at 64KB/inst
System Cache	4x 16 instances (double size)  <b>8MB</b> at 128KB/inst	2x 32 instances  <b>4MB</b> at 64KB/inst

Note that [typically, cache sizes were doubled](#), except of the L2 caches of the big cores.

### 13. Apple A12 with dual big and quad LITTLE cores (8)

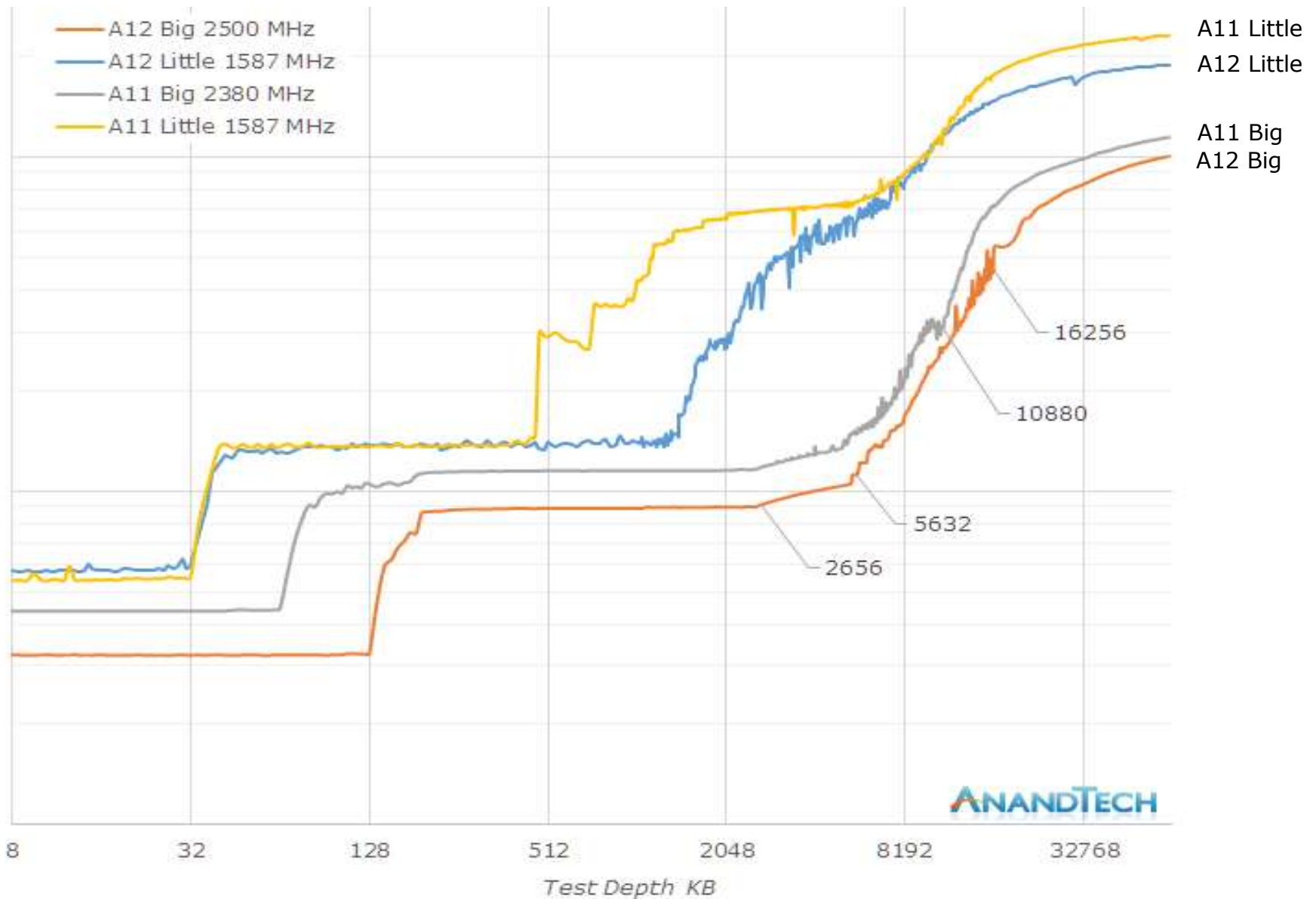
Full random latency of A12 caches vs. A11 caches (linear scale) [64]





## 13. Apple A12 with dual big and quad LITTLE cores (9)

Full random latency of A12 caches vs. A11 caches (log scale) [64]





## 13. Apple A12 with dual big and quad LITTLE cores (10)

### b) Improved Neural Engine

As long as the Neural Engine of the A11 is a dual-core design with up to 600 billion operation per sec., the advanced Neural Engine of the A12 is an eight-core design with up to 5 trillion operations per sec.

## 13. Apple A12 with dual big and quad LITTLE cores (11)

### The Core ML machine learning framework of Apple [66]

- It is used on Apple's devices (macOS, iOS, watchOS, and tvOS) to convert trained ML models, created with third-party ML tools, like XGBoost, Keras, LibSVM, scikit-learn or Facebook's Caffe and Caffe2, to the Core ML model format and let perform fast prediction or inference on the Apple device.
- Apple introduced Core ML in 06/2017.
- In 12/2017 Google released a tool that converts AI models produced using TensorFlow Lite into a file type compatible with Apple's Core ML.

### 13. Apple A12 with dual big and quad LITTLE cores (12)

Programming frameworks used to create ML models [67]



## 13. Apple A12 with dual big and quad LITTLE cores (13)

### Remarks

- Neon: Intel (originally from Nervana Systems, Python based), released: 05/2015
- TensorFlow: Google, released 11/2015
- Caffe: Facebook, originally developed at U. of California, Berkeley, release vo: 12/2013
- Caffe2: Facebook, 04/2017
- Caffe2 Go: Facebook, 10/2017
- MXNet (originated at the Carnegie Mellon U. and U. of Washington.  
It is now developed in cooperation by multiple universities and companies, including Amazon, Baidu, Intel, Microsoft and Nvidia.  
Supports building and training models in Python, R, Scala, Julia, and C++).

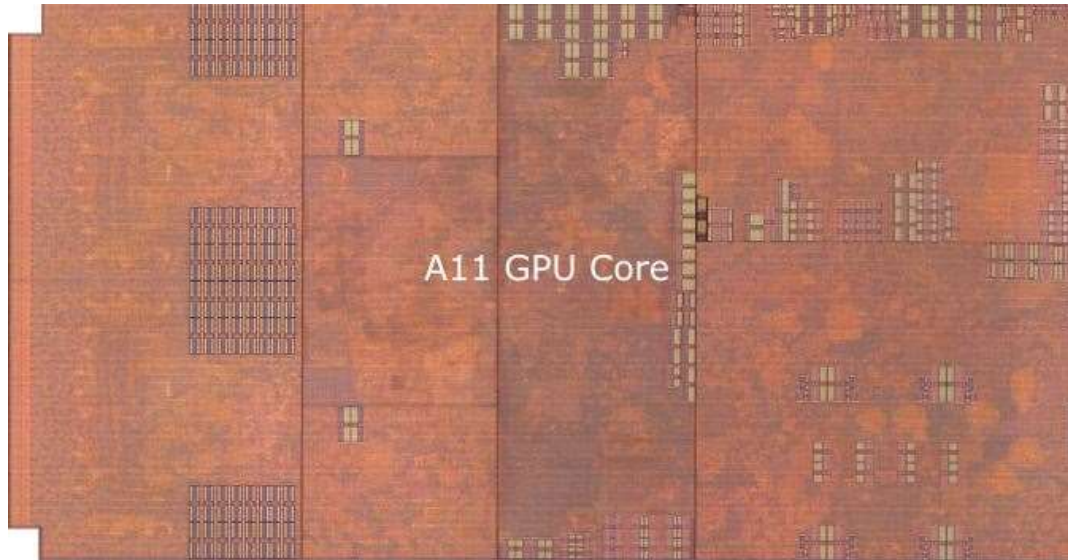
## 13. Apple A12 with dual big and quad LITTLE cores (14)

### c) Improved GPU [64]

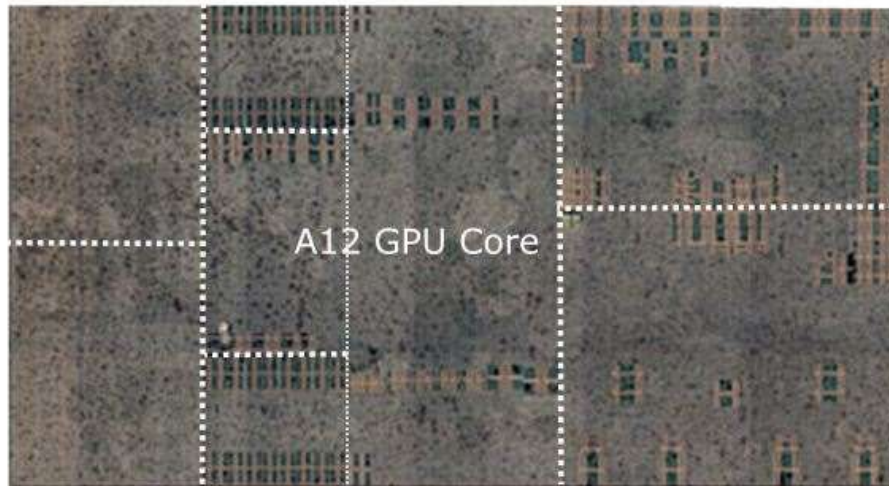
- The 3-core GPU of the A11 was Apple's first in-house design, it resembles to the previous Imagination design.
- A12's GPU has 4 cores and still looks similar to the Imagination design.

### 13. Apple A12 with dual big and quad LITTLE cores (15)

Contrasting the floor plans of the GPUs of A11 and A12 [64]



3-core  
design



4-core  
design

## 13. Apple A12 with dual big and quad LITTLE cores (16)

Major innovation: Lossless memory compression of data transfers between the frame buffer and main memory

- **Frame buffer compression** is a **widely used** technique in GPUs **to reduce bandwidth and power consumption while transferring data between the frame buffer and the main memory** for years.
- It is utilized both in discrete GPUs of desktop processors and integrated GPUs of desktops or mobiles by vendors like Nvidia, AMD, Qualcomm or Imagination Technologies.
- In order to give a glimpse into this technique subsequently we briefly describe **ARM's AFBC (ARM Frame Buffer Compression)** method.



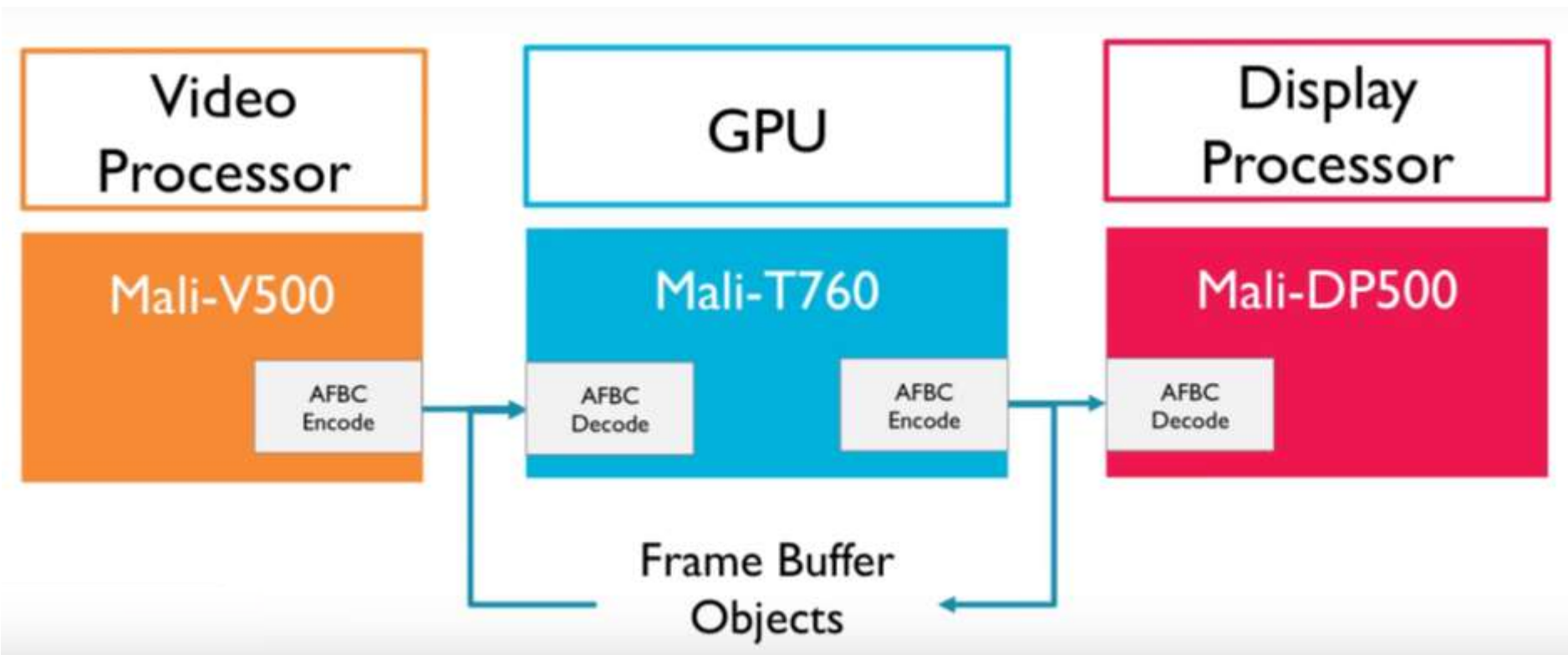
## 13. Apple A12 with dual big and quad LITTLE cores (17)

### Principle of operation [68]

If a portion, portions or the whole image frame is detected as being relatively static (i.e. unchanged or changeless regarding to a threshold) for a period of time larger than a given threshold, AFBC will be applied.

### 13. Apple A12 with dual big and quad LITTLE cores (18)

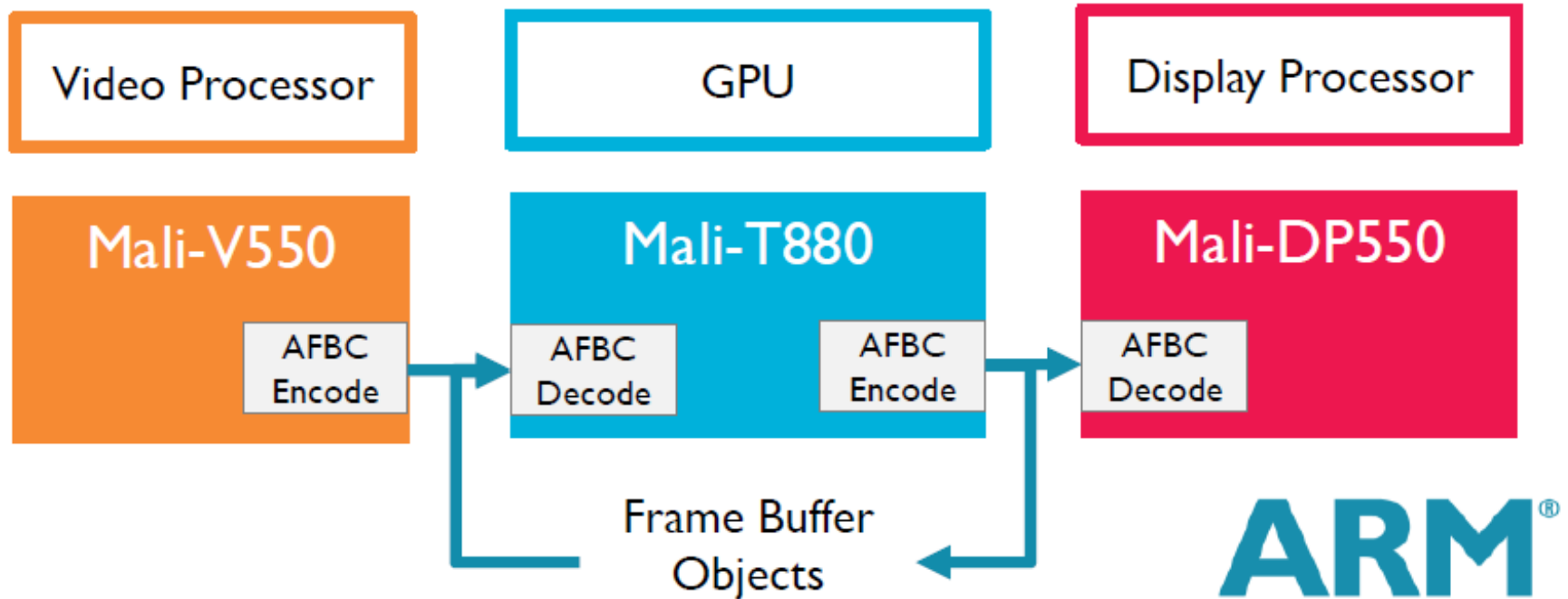
First implementation of ARM's AFBC technique (2013) [69]



### 13. Apple A12 with dual big and quad LITTLE cores (19)

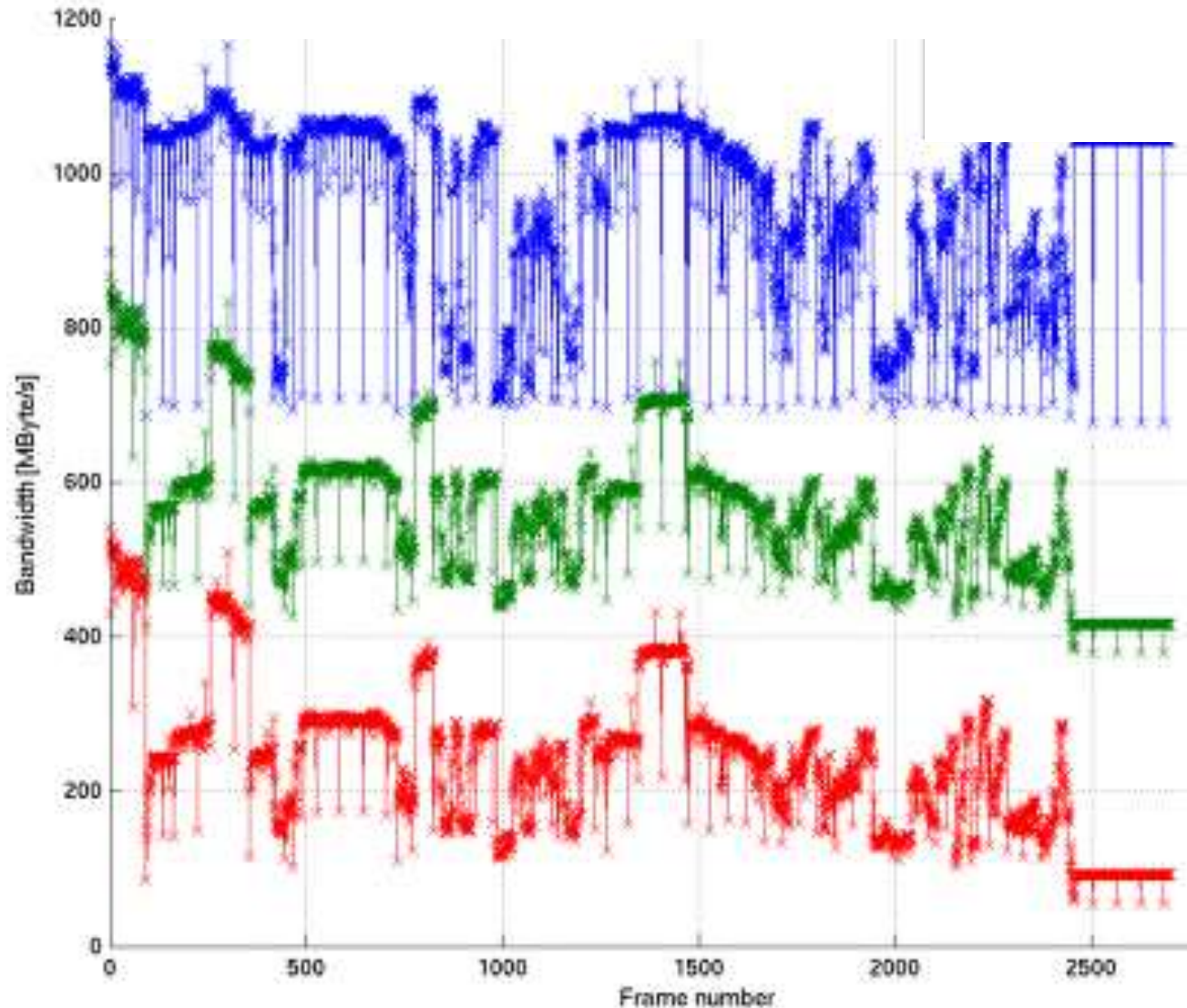
Implementation of ARM's AFBC technique in the Mali T800 GPUs (2015) [70]

#### AFBC integration with media system



### 13. Apple A12 with dual big and quad LITTLE cores (20)

Bandwidth reduction by AFBC while decoding a 4K H.264 video stream [69]



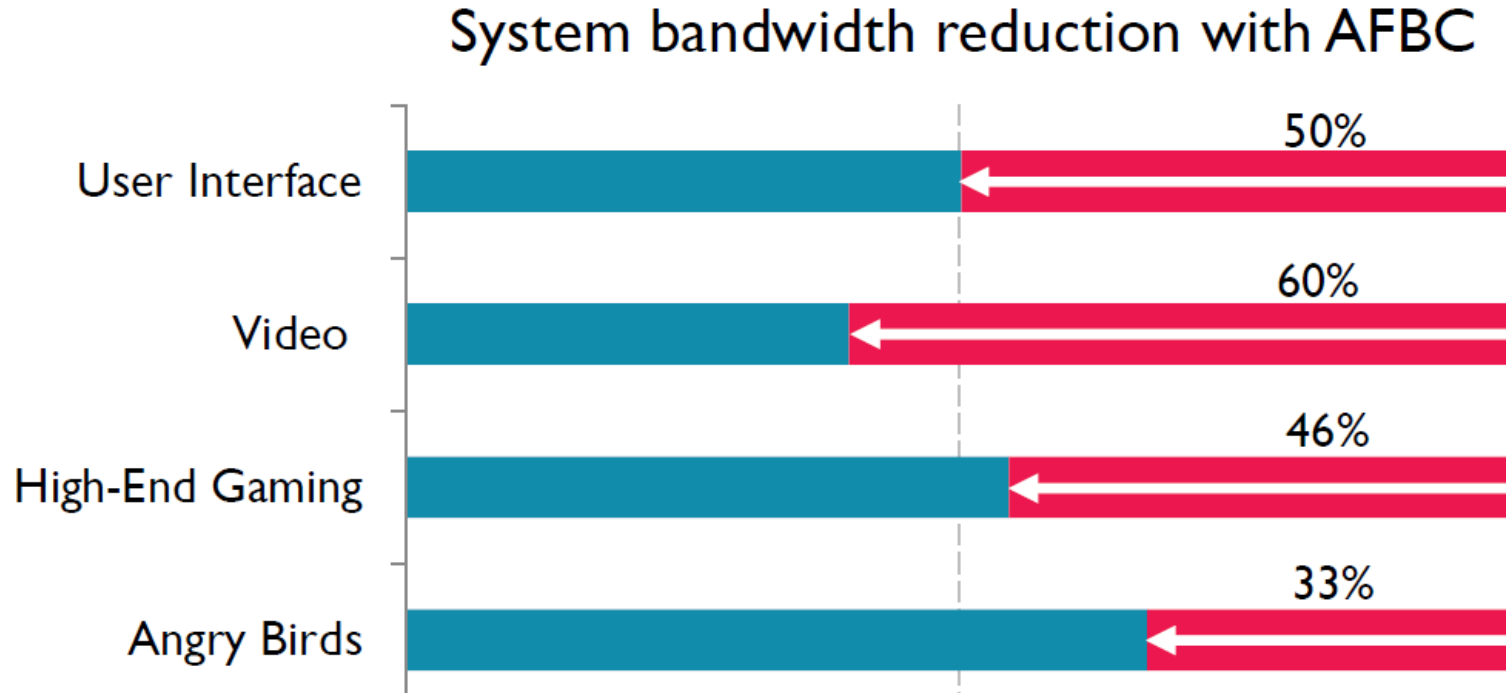
No AFBC

AFBC is used for  
internal reference  
frame compression  
only

AFBC compression is  
used for the output  
frame as well

### 13. Apple A12 with dual big and quad LITTLE cores (21)

System bandwidth reduction achieved by ARM's AFBC technique [70]



## 13. Apple A12 with dual big and quad LITTLE cores (22)

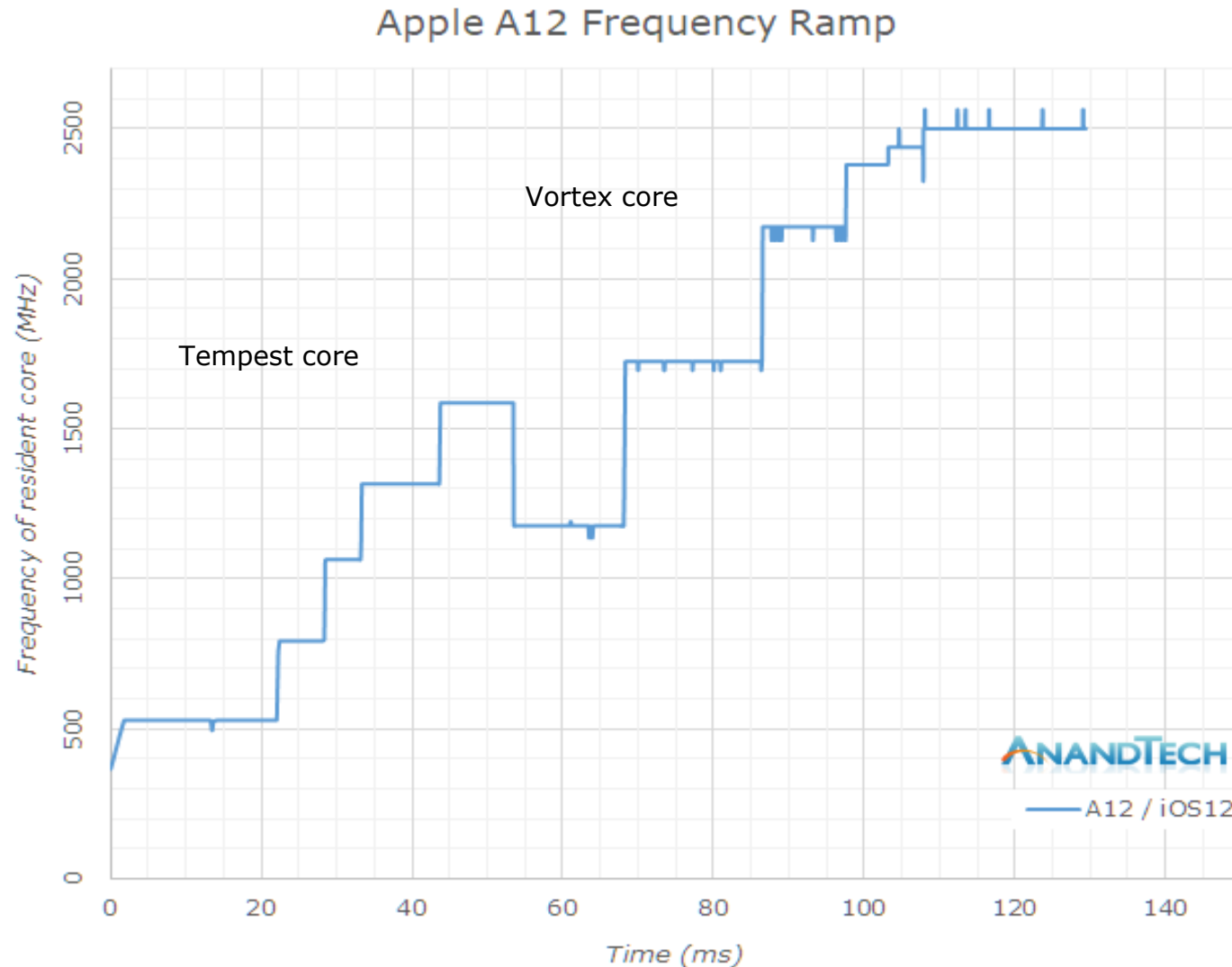
### Remarks

ARM enhanced their AFBC to **AFBC 1.2** by introducing some optimizations in 2016 (first implemented in the Mali G51 GPU).

Apple introduced **frame buffer compression** relatively late, in 2018 along with the A12 processor.

### 13. Apple A12 with dual big and quad LITTLE cores (23)

Load ramping (tracking frequency over time in a workload from idle to full performance in the A12 [64])





# 13. Apple A12 with dual big and quad LITTLE cores (24)

## SPEC2006 energy efficiency estimate [64]

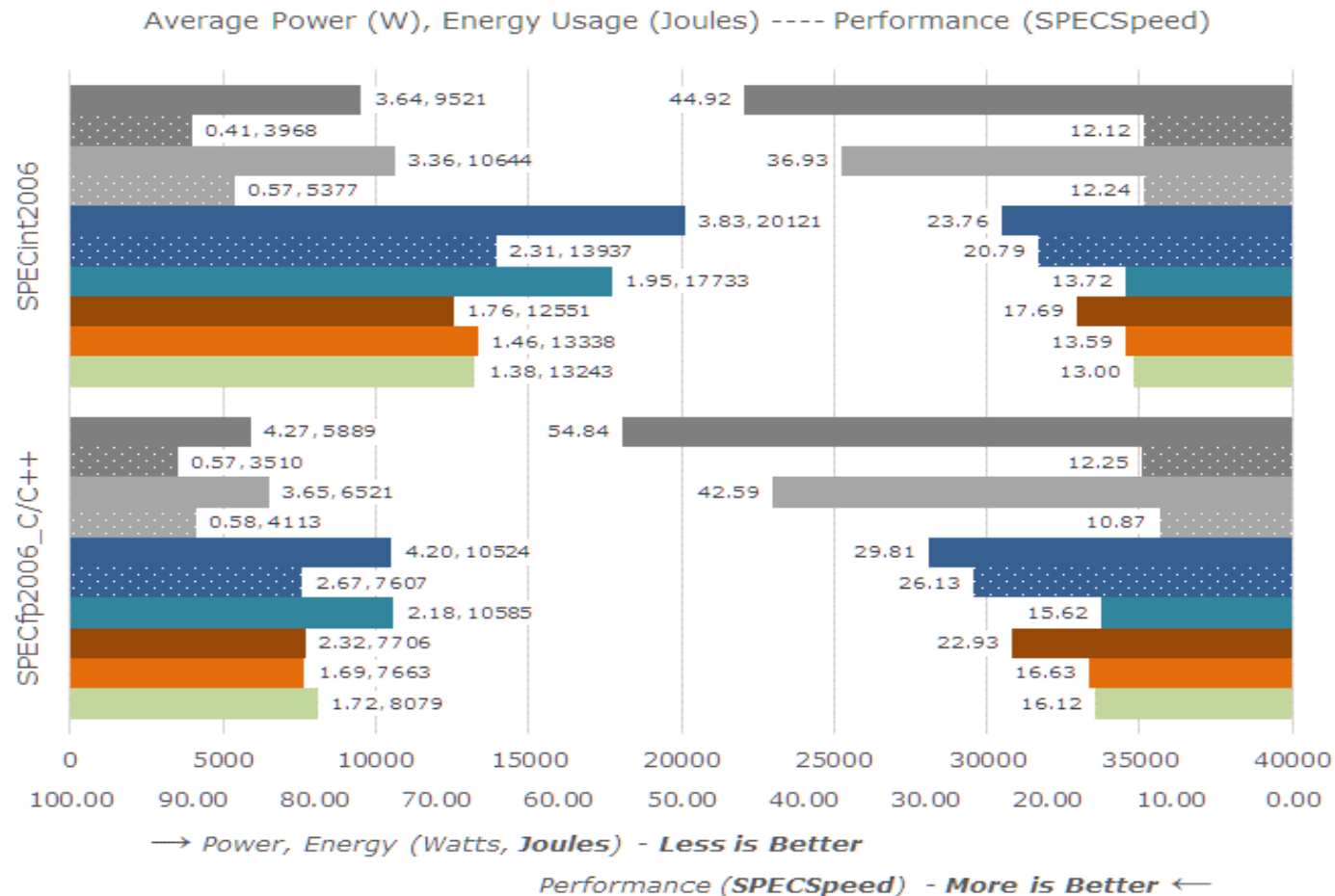
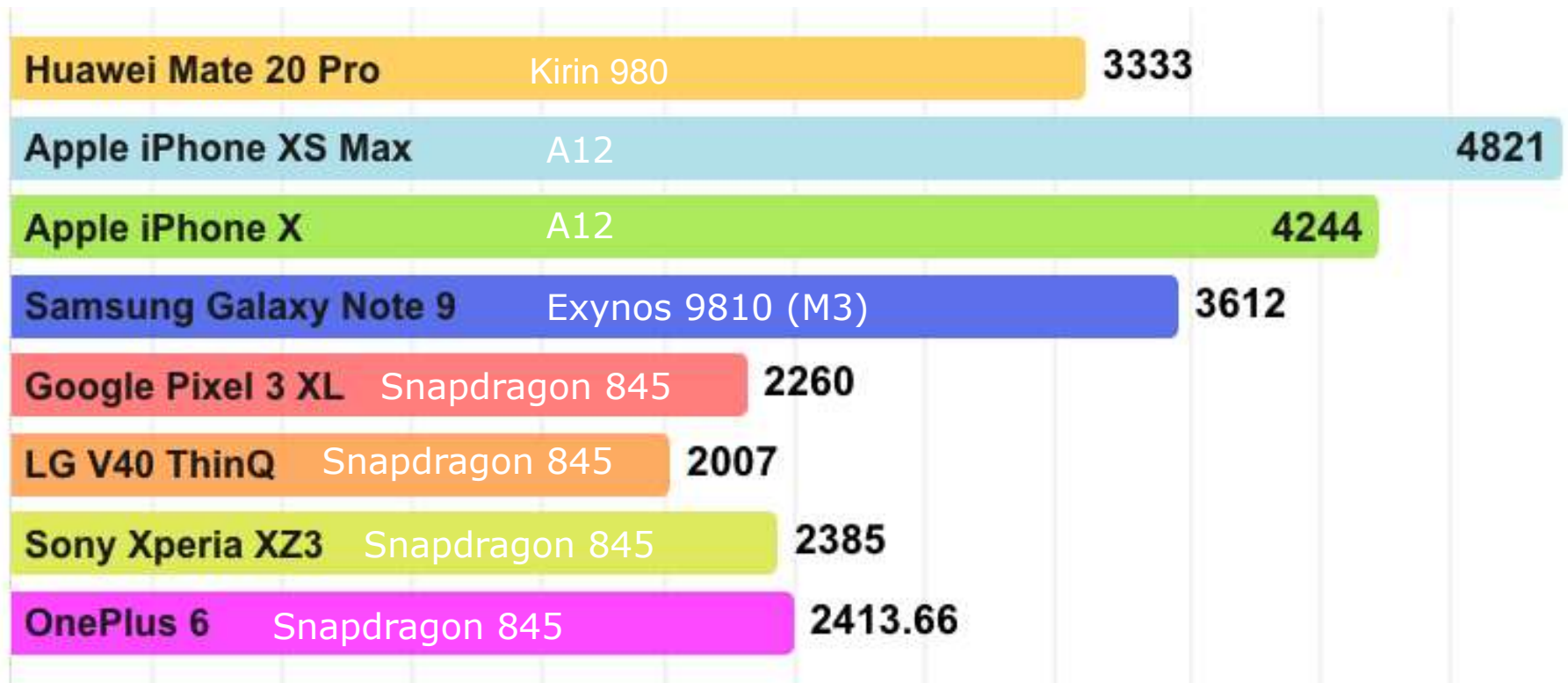


Chart series order in same order as legend order

### 13. Apple A12 with dual big and quad LITTLE cores (25)

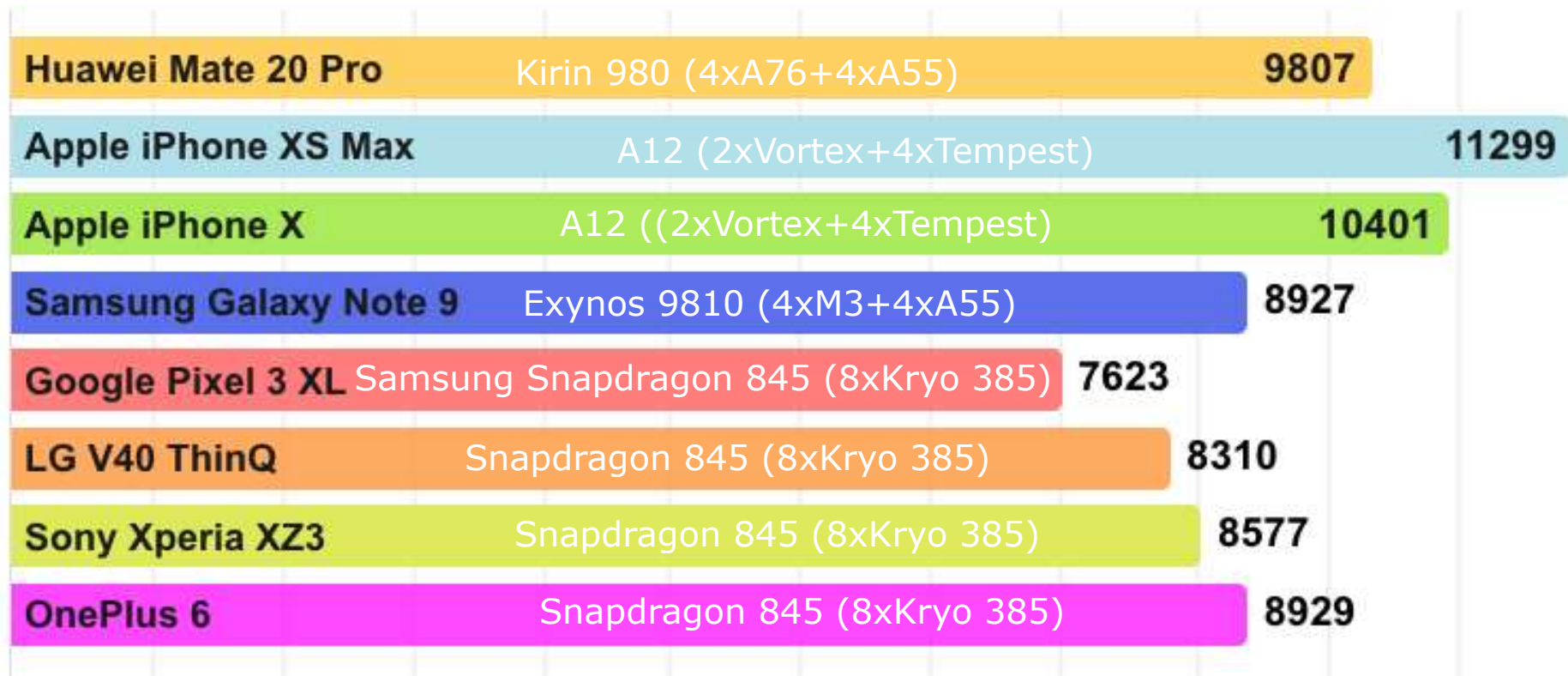
-Single-core GeekBench 4 scores of select processors [71]



Note the outstanding single core performance of the A12.

### 13. Apple A12 with dual big and quad LITTLE cores (26)

Multi-core GeekBench 4 scores of select processors [71]



Note again the **outstanding multi-core performance of the dual-core A12 processors vs. processors with 4 big cores** (the Snapdragon 845 has 4 high-performance Kryo 385 cores running at up to 2.8 GHz and 4 efficient Kryo 385 cores running at up to 1.8 GHz).

14. Apple A12X with quad big and quad LITTLE cores






## 14. Apple A12X with quad big and quad LITTLE cores (1)

### 14. Apple A12X with quad big and quad LITTLE cores [72]

- Released in **10/2018** in the 11" iPad Pro 11" and the 12.9" iPad Pro.
- These tablet models are also called the **3. generation iPad Pro models**.
- The A12X is manufactured by **7 nm technology** by TSMC as a PoP package with **up to 6 GB LPDDR4x** memory.
- Transistor count: 10 **billion**.
- The A12 provides **about 30 % more single core performance and about 90 % more multi-core performance** compared to the A10X, as GeekBench 4 data presented subsequently, show.

# 14. Apple A12X with quad big and quad LITTLE cores (2)

## Main features of the A12X Bionic SoC

Appl. proc.S6	Model no.	Image	Node	Die size	CPU	CPU ISA	CPU cache (big core)	GPU	Memory (Up to)	Intro.	Utilizing devices
<b>A10 (Fusion)</b>	APL1W24		16 nm FinFET	125 mm <sup>2</sup>	2xHurricane (2.34 GHz)+ 2x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 3 MB LS: 4 MB	PowerVR GT7600 Plus (6C) @ >650 MHz (>250 GFLOPS) (redesigned)	2 GB/3 GB LPDDR4x	9/2016	iPhone 7 iPhone 7 Plus
<b>A10X (Fusion)</b>	APL1071 (TSMC)		10 nm FinFET	96.4 mm <sup>2</sup>	3xHurricane (2.38 GHz)+ 3x Zephyr (1.1 GHz?)	ARM v8-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: none	PowerVR GT7600 Plus (12C)	3 GB/4 GB LPDDR4x	6/2017	iPad Pro 10.5" iPad Pro 12.9" Apple TV 4K
<b>A11 Bionic</b>	APL1W72 (TSMC)		10 nm FinFET	88 mm <sup>2</sup>	2x Monsoon (2.38 GHz) + 4x Mistral (1.69 GHz)	ARM V8.2-A	L1i: 64 KB L1d: 64 KB L2: 8 MB LS: 4 MB	Apple Custom GPU (3C)	2 GB/3 GB? LPDDR4x	9/2017	iPhone 8 iPhone 8 Plus iPhone X
<b>A12 Bionic</b>	APL1W82 (TSMC)		7 nm FinFET	83 mm <sup>2</sup>	2x Vortex (2.50 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (4C)	3 GB/4 GB LPDDR4X	9/2018	iPhone XS 5.8" iPhone XS Max iPhone XR 6.1"
<b>A12X Bionic</b>	APL1083 (TSMC)		7 nm FinFET	122 mm <sup>2</sup>	4x Vortex (2.48 GHz) + 4x Tempest (1.59 GHz)	ARM V8.3-A	L1i: 128 KB L1d: 128 KB L2: 6 MB/core LS: 8 MB	Apple Custom GPU (7C)	6 GB LPDDR4X	10/2018	iPad Pro 11" iPad Pro 12.9"

LS: System cache, it services the entire SoC

## 14. Apple A12X with quad big and quad LITTLE cores (3)

### Main enhancements of the A12X versus the A12 [72]

- The A12X has a 7-core GPU vs. 4 cores implemented in the A12.  
This graphics performance is claimed to be equivalent to that of the Xbox One S.
- In the A12X the new task scheduler (called performance controller) allows all CPU cores to run simultaneously (inclusive core allocation) rather than the big and little cores exclusively.

This new performance controller is used also along with the A12.



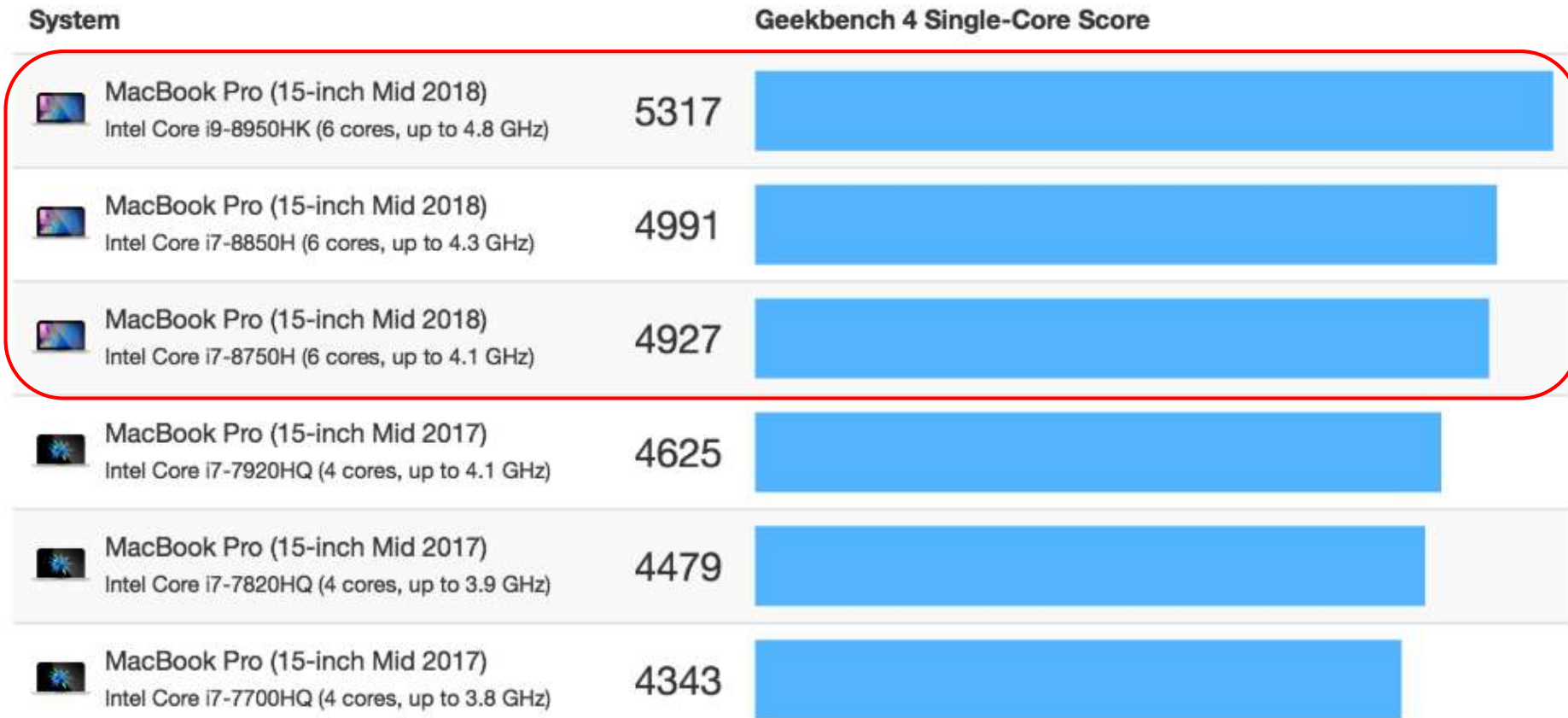
## 14. Apple A12X with quad big and quad LITTLE cores (4)

### Contrasting GeekBench 4 scores of Intel processor-based MacBook DTs with A12X-based iPad Pro tablets -1

- Recent MacBooks are based on Intel's high performance i9 or i7 processors, like the 15" MacBook Pro on the i9-8950HK processor.
- Even so, the performance of Apple's in-house developed A12X, used in the iPad Pro tablets, approaches more and more the performance of Intel's advanced DT processors, used in Apple's MacBooks, as indicated in the next Figures.

## 14. Apple A12X with quad big and quad LITTLE cores (5)






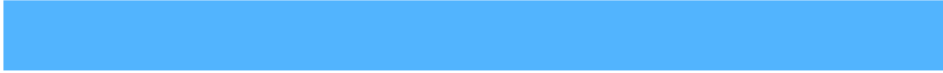





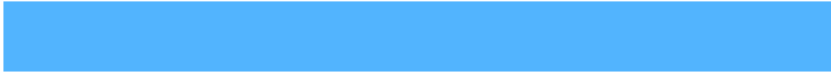








GeekBench 4 Single-core scores for MacBook Pro (15") DTs [73]



Source: Geekbench 4 <http://www.geekbench.com/>

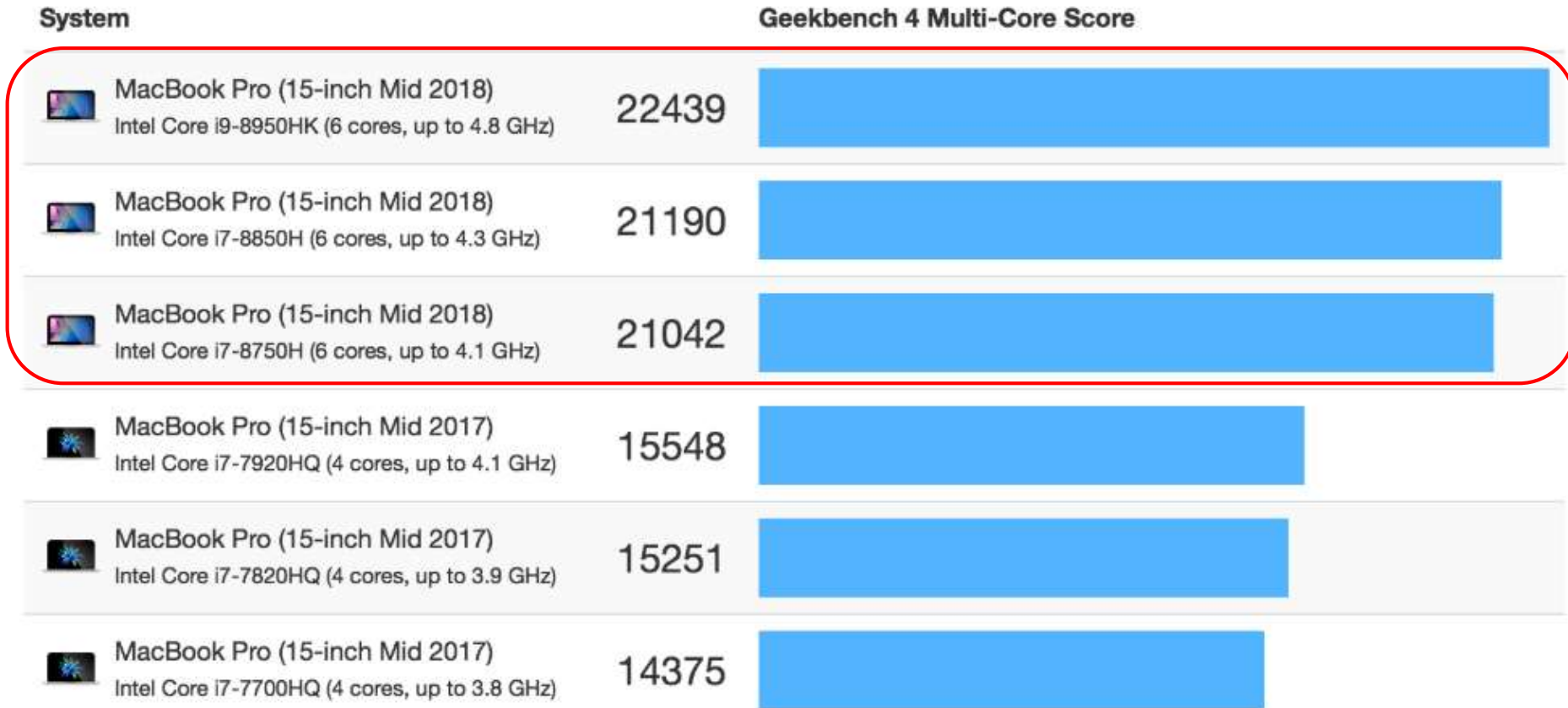
## 14. Apple A12X with quad big and quad LITTLE cores (6)

GeekBench 4 Single-core scores for iPad Pro tablets and iPhone mobiles [74]

Device	Score	
 <b>iPad Pro (11-inch)</b> Apple A12X Bionic @ 2.5 GHz	5005	
 <b>iPad Pro (12.9-inch 3rd Generation)</b> Apple A12X Bionic @ 2.5 GHz	5005	
 <b>iPhone XS Max</b> Apple A12 Bionic @ 2.5 GHz	4797	
 <b>iPhone XS</b> Apple A12 Bionic @ 2.5 GHz	4796	
 <b>iPhone XR</b> Apple A12 Bionic @ 2.5 GHz	4795	
 <b>iPhone 8</b> Apple A11 Bionic @ 2.4 GHz	4224	
 <b>iPhone 8 Plus</b> Apple A11 Bionic @ 2.4 GHz	4222	
 <b>iPhone X</b> Apple A11 Bionic @ 2.4 GHz	4213	
 <b>iPad Pro (10.5-inch)</b> Apple A10X Fusion @ 2.3 GHz	3915	
 <b>iPad Pro (12.9-inch 2nd Generation)</b> Apple A10X Fusion @ 2.3 GHz	3911	

## 14. Apple A12X with quad big and quad LITTLE cores (7)











### GeekBench 4 Multi-core scores for MacBook Pro (15") DTs [73]



Source: Geekbench 4 <http://www.geekbench.com/>

## 14. Apple A12X with quad big and quad LITTLE cores (8)

GeekBench 4 Multi-core scores for iPad Pro tablets and iPhone mobiles [74]

Device	Score	
 iPad Pro (12.9-inch 3rd Generation) Apple A12X Bionic @ 2.5 GHz	17920	<div></div>
 iPad Pro (11-inch) Apple A12X Bionic @ 2.5 GHz	17879	<div></div>
 iPhone XS Apple A12 Bionic @ 2.5 GHz	11258	<div></div>
 iPhone XR Apple A12 Bionic @ 2.5 GHz	11208	<div></div>
 iPhone XS Max Apple A12 Bionic @ 2.5 GHz	11203	<div></div>
 iPhone 8 Plus Apple A11 Bionic @ 2.4 GHz	10185	<div></div>
 iPhone X Apple A11 Bionic @ 2.4 GHz	10145	<div></div>
 iPhone 8 Apple A11 Bionic @ 2.4 GHz	10140	<div></div>
 iPad Pro (10.5-inch) Apple A10X Fusion @ 2.3 GHz	9338	<div></div>
 iPad Pro (12.9-inch 2nd Generation) Apple A10X Fusion @ 2.3 GHz	9321	<div></div>

## 14. Apple A12X with quad big and quad LITTLE cores (9)

Geekbench 4 scores of Intel's 15 W i7-xxxxU processors [75]

Model	CPU cores	Launched	GB 4 SC max	GB 4 MC max	Family	Techn.
I7-4500U	2C	6/2013	3854	6854	Haswell	22 nm
I7-4600U	2C	9/2013	4202	7592	Haswell	22 nm
i7-5600U	2C	1/2015	4217	8018	Broadwell	14 nm
I7-6600U	2C	9/2015	4775	9010	Skylake	14 nm
I7-7560U	2C	8/2016	5000	10182	Kaby Lake	14 nm
I7-7660U	2C	1/2017	5128	10389	Kaby Lake	14 nm
I7-8565U	4C	8/2018	5576	17813	Coffee Lake	14 nm

## 14. Apple A12X with quad big and quad LITTLE cores (10)

Geekbench 4 scores of Apple's A series processors [74]

Model	CPU cores	Launched	GB 4 SC max	GB 4 MC max	Techn.
A8	2C	9/2014	1663	2855	20 nm
A8X	3C	10/2014	1798	4214	20 nm
A9	2C	9/2015	2524	4391	14/16 nm
A9X	2C	11/2015	3057	5114	16 nm
A10	2+2C	9/2016	3480	5928	16 nm
A10X	3+3C	6/2017	3915	9339	10 nm
A11	2+4C	9/2017	4224	10185	10 nm
A12	2+4C	9/2018	4797	11260	7 nm
A12X	4+4C	10/2018	5006	17925	7 nm



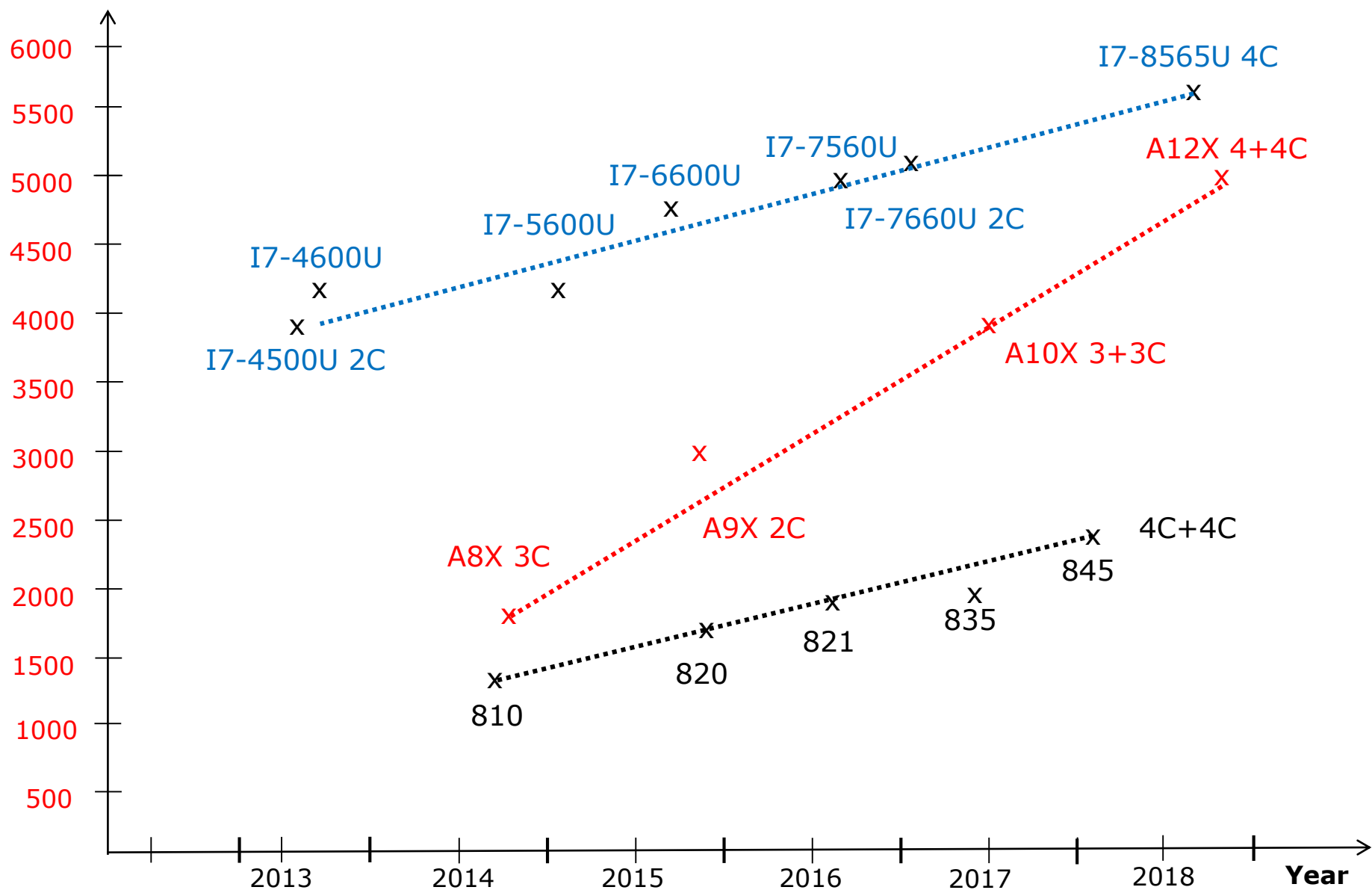
## 14. Apple A12X with quad big and quad LITTLE cores (11)

Geekbench 4 scores of Qualcomm's Snapdragon processors [76]

Model	CPU cores	Launched	GB 4 SC max	GB 4 MC max	Techn.
808	2+4C	Q3/2014	1152	2813	20 nm
810	4+4C	Q3/2014	1351	3446	20 nm
820	4+4C	Q4/2015	1702	3955	14 nm
821	4+4C	Q3/2016	1880	4430	14 nm
835	4+4C	Q2/2017	1947	6624	10 nm
845	4+4C	Q1/2018	2415	8689	10 nm
850	4+4C	Q3/2018			10 nm
855	1+3+4C	Q1/2019			7 nm

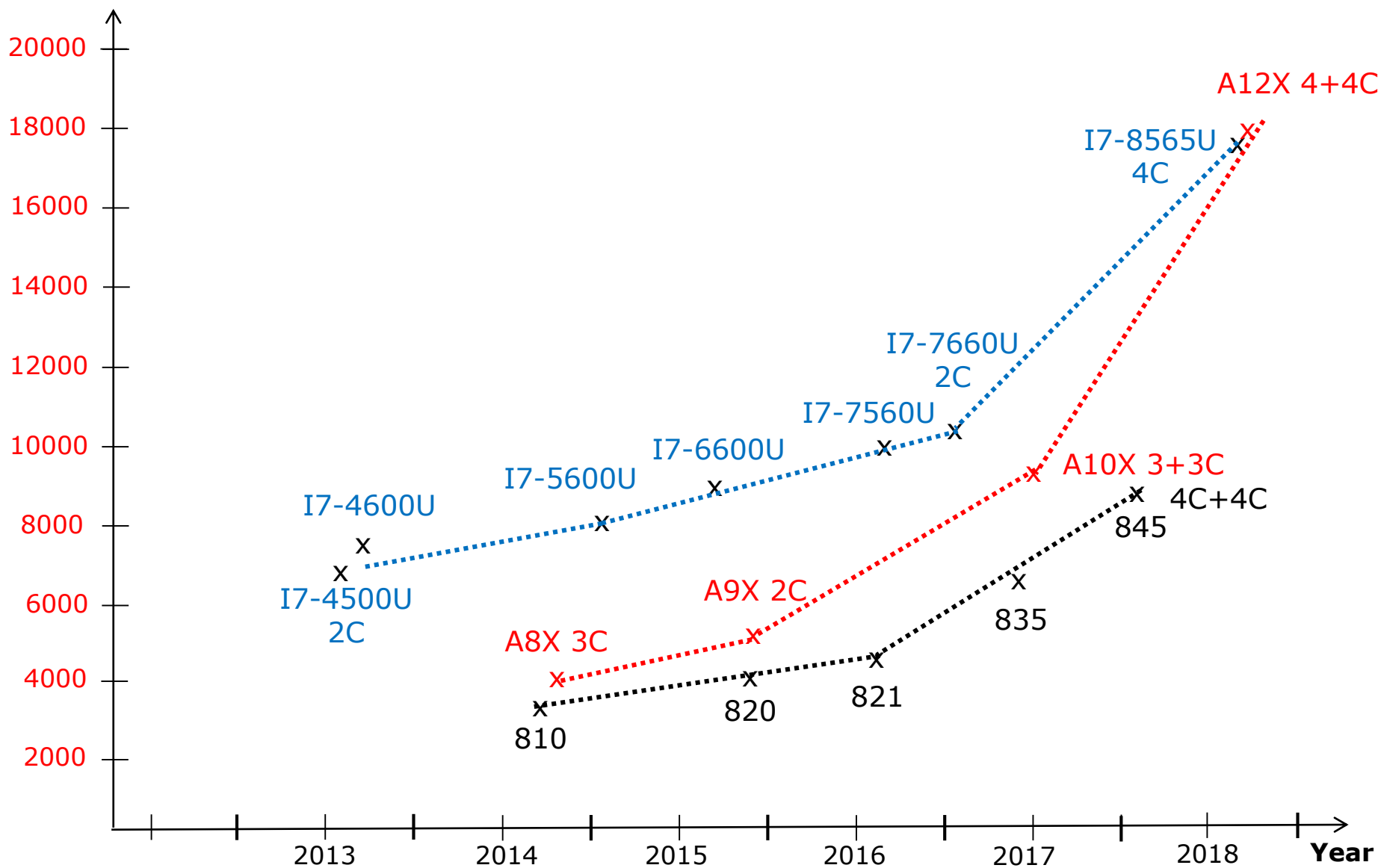
## 14. Apple A12X with quad big and quad LITTLE cores (12)

Geekbench 4 SC scores of Intel's, Apple's and Qualcomm's processors



## 14. Apple A12X with quad big and quad LITTLE cores (13)

Geekbench 4 MC scores of Intel's, Apple's and Qualcomm's processors



## 14. Apple A12X with quad big and quad LITTLE cores (14)

### Contrasting GeekBench 4 scores of Intel processor-based MacBook DTs with A12X-based iPad Pro tablets -2

- A comparison of the A10X and A12X performance scores indicates a massive evolution of the GeekBench 4 scores of Apple's AxxX processors.

This fast improvement in performance figures lets suggest that [Apple is expected to replace soon Intel's processors by in-house developed AxxX processors in their MacBooks.](#)

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