MediaTek's mobile processor lines

Dezső Sima

Vers. 3.0

Januar 2019

MediaTek's mobile processor lines

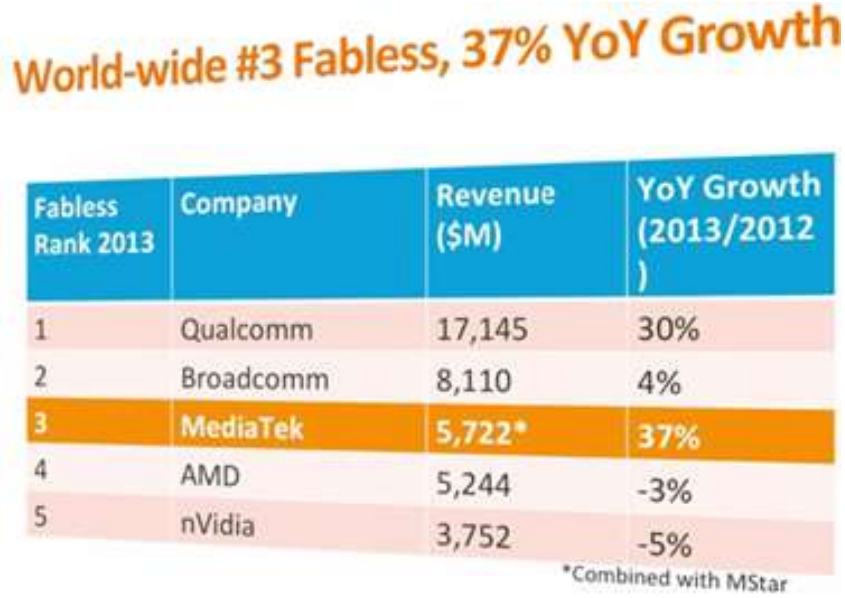
- 1. MediaTek's mobile processors
- 2. MediaTek’s smartphone processors
- 3. MediaTek’s tablet processors
- 4. MediaTek’s CorePilot task scheduler
- 5. References

1. Overview

1. Overview

Introduction to the company MediaTek-1

- It is a fabless Taiwanese chipmaker, founded in 1997.
- MediaTek designed first chipsets for home entertainment devices, such as DVDs, digital TVs and subsequntly also for mobile phones and tables.
- In 2013 MediaTek became the 10. largest semiconductor company and the third largest fabless semiconductor company, as indicated below.



World-wide #3 Fabless, 37% YoY Growth

Fabless Rank 2013	Company	Revenue ($M)	YoY Growth (2013/2012)
1	Qualcomm	17,145	30%
2	Broadcomm	8,110	4%
3	MediaTek	5,722*	37%
4	AMD	5,244	-3%
5	nVidia	3,752	-5%

*Combined with MStar

MediaTek's global ranking among fabless semiconductor companies in 2013 [2]

Introduction to the company MediaTek-2

- MediaTek achieved an exponential growth in selling chipsets from 10 million in 2011 to about 350 million in 2014 [1].

  In the Chinese smartphone market MediaTek achieved even over 50 % market share in 2013 mainly due to their integrated processor-baseband modem design.

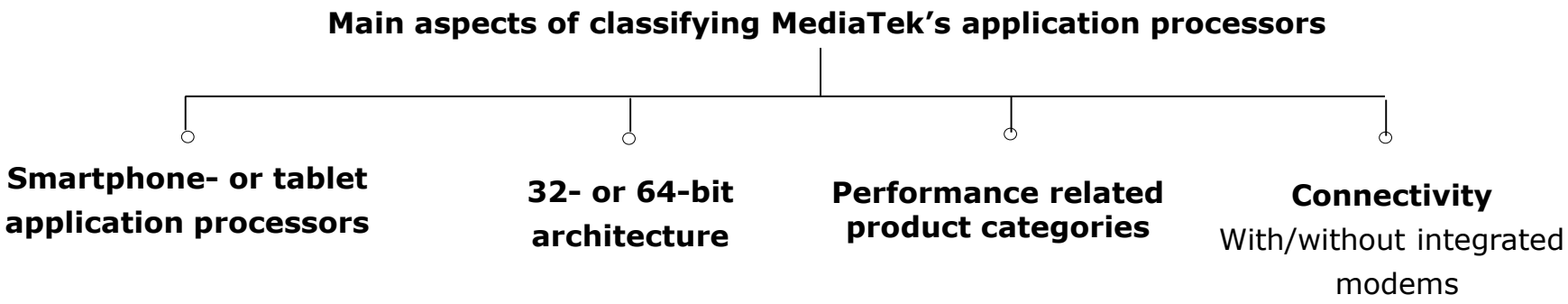
- In 2015 MediaTek had the third position in the worldwide market share of smartphone application processors, as the Table below on the left side indicates.

Smartphone application processors worldwide market share 2015 (revenue)	
Qualcomm (USA)	42 %
Apple (USA)	21 %
MediaTek (Taiwan)	19 %
Samsung (S. Korea)	
Spreadtrum (China)	

Tablet application processors worldwide market share 2015 (revenue)	
Apple (USA)	31 %
Qualcomm (USA)	16 %
Intel (USA)	14 %
MediaTek (Taiwan)	
Samsung (S. Korea)	

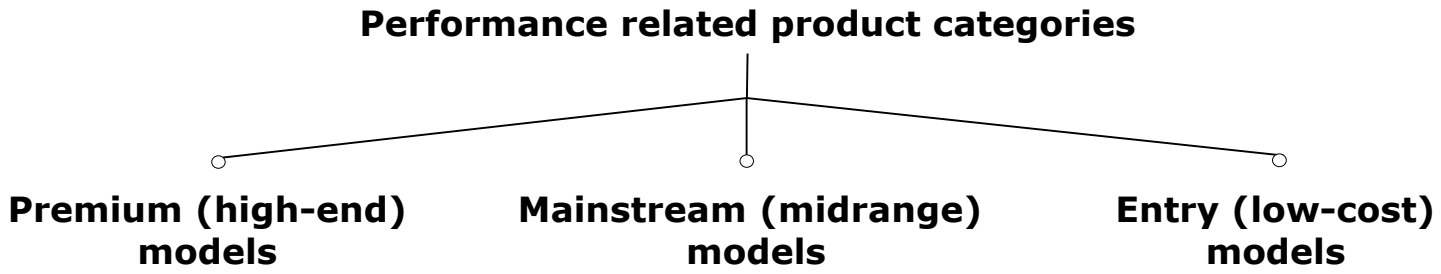
Table: Worldwide market share of smarphone and tablet application processors in 2015 (based on revenue) [Source: Press releases of Strategy Analytics]

Main aspects of classifying MediaTek's application processors



Performance related product categories of Mediatek's application processors

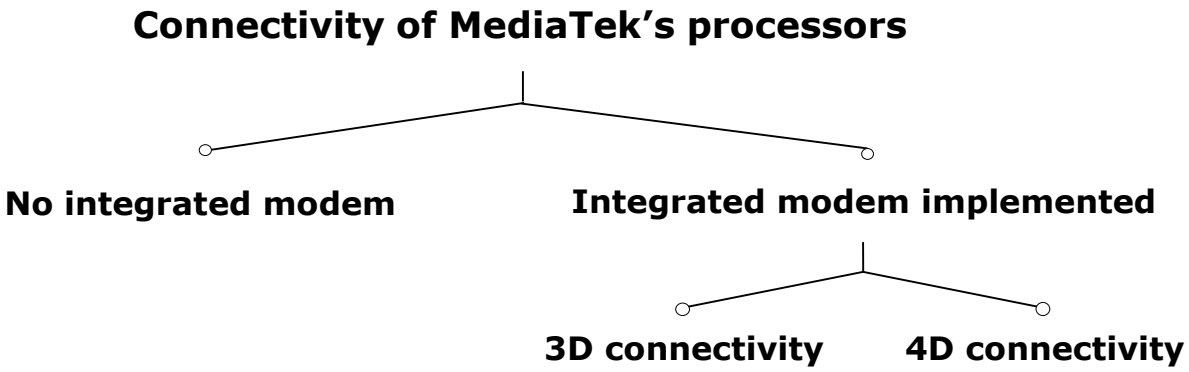
According to their performance features MediaTek deifferentiates between three performance related product categories, as indicated below.



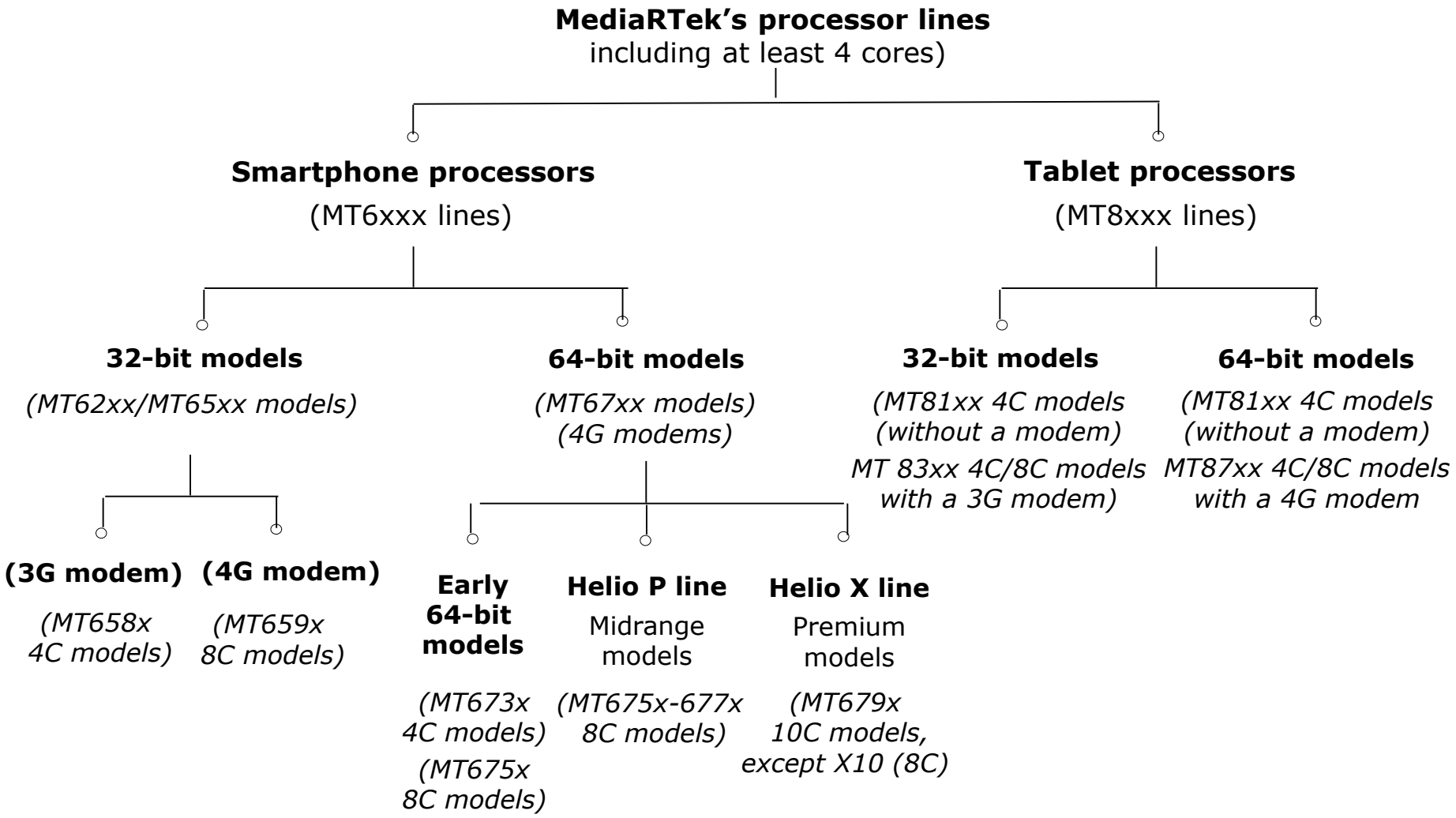
As an example for this categorization see MediaTek’s smartphone product roadmap for 2014-2015 in the next Figure.

MediaTek's performance related product categories, exemplified by their smartphone product roadmap 2014-2015 [24]

Connectivity of MediaTek's processors



Overview of MediaTek's processor lines



2. MediaTek’s smartphone processors

- 2.1 Overview
- 2.2 MediaTek’s 32-bit smartphone processors
- 2.3 MediaTek’s 64-bit smartphone processors

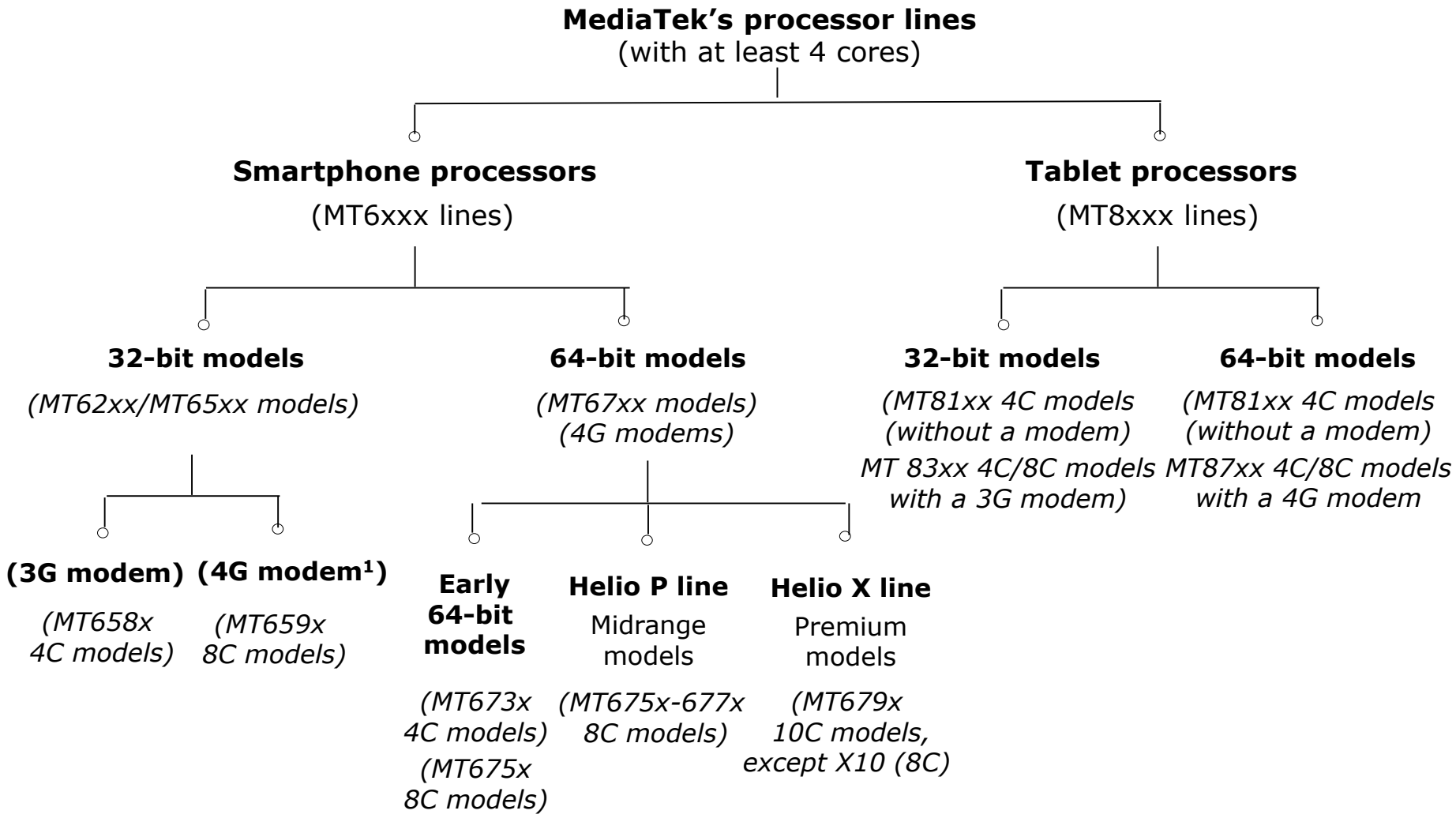
2.1 Overview

2. MediaTek’s smartphone processors

2.1 Overview

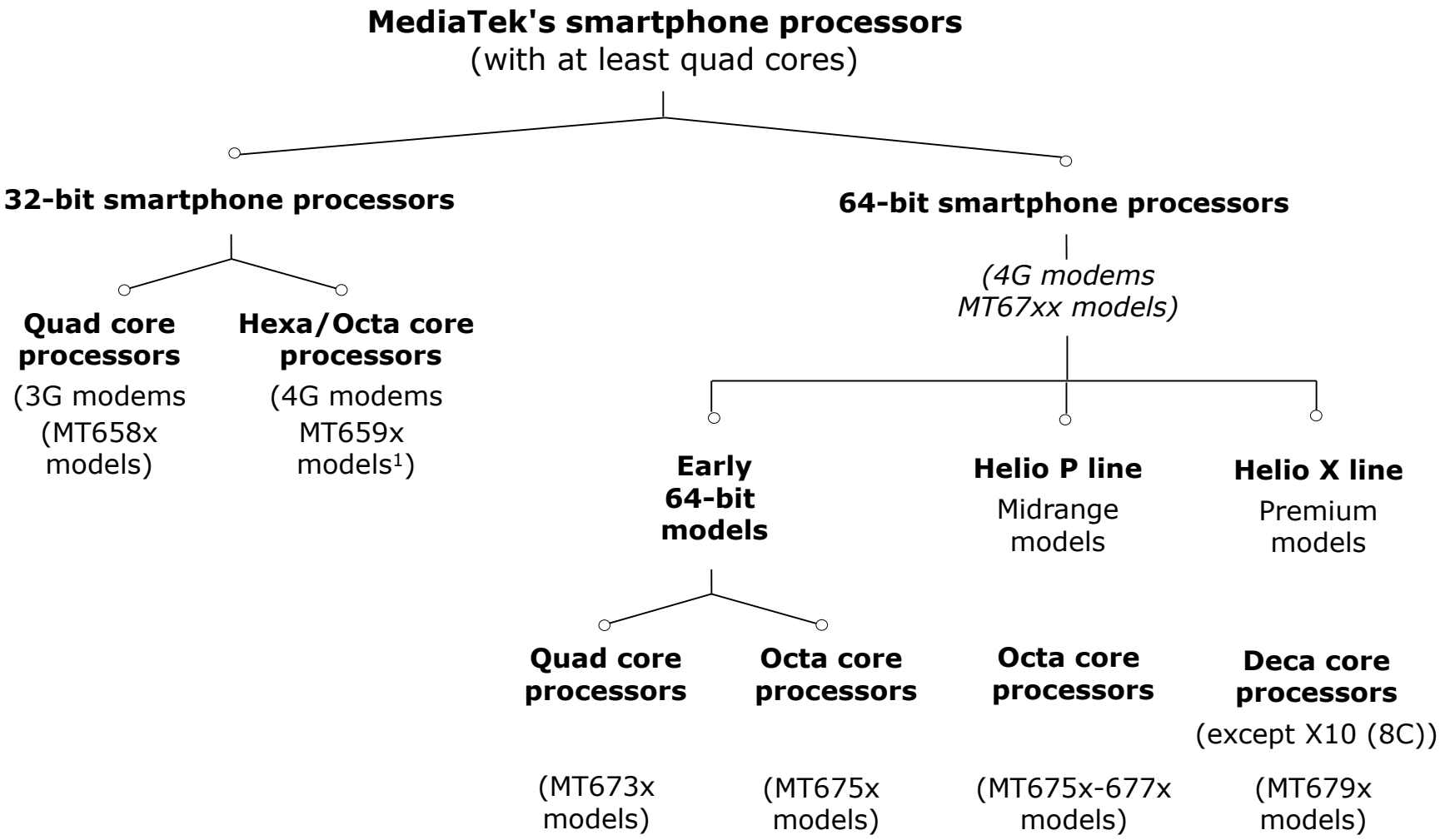
- MediaTek designs and sales smartphone application processsors since about 2009.
- Subsequently, first we give an overview of MediaTek's 32-bit (at least) quad-core smartphone application processors followed by the 64-bit smartphone SoCs.

Overview of MediaTek's processor lines



[1]The MT6591/MT6592 models need an external modem to provide LTE

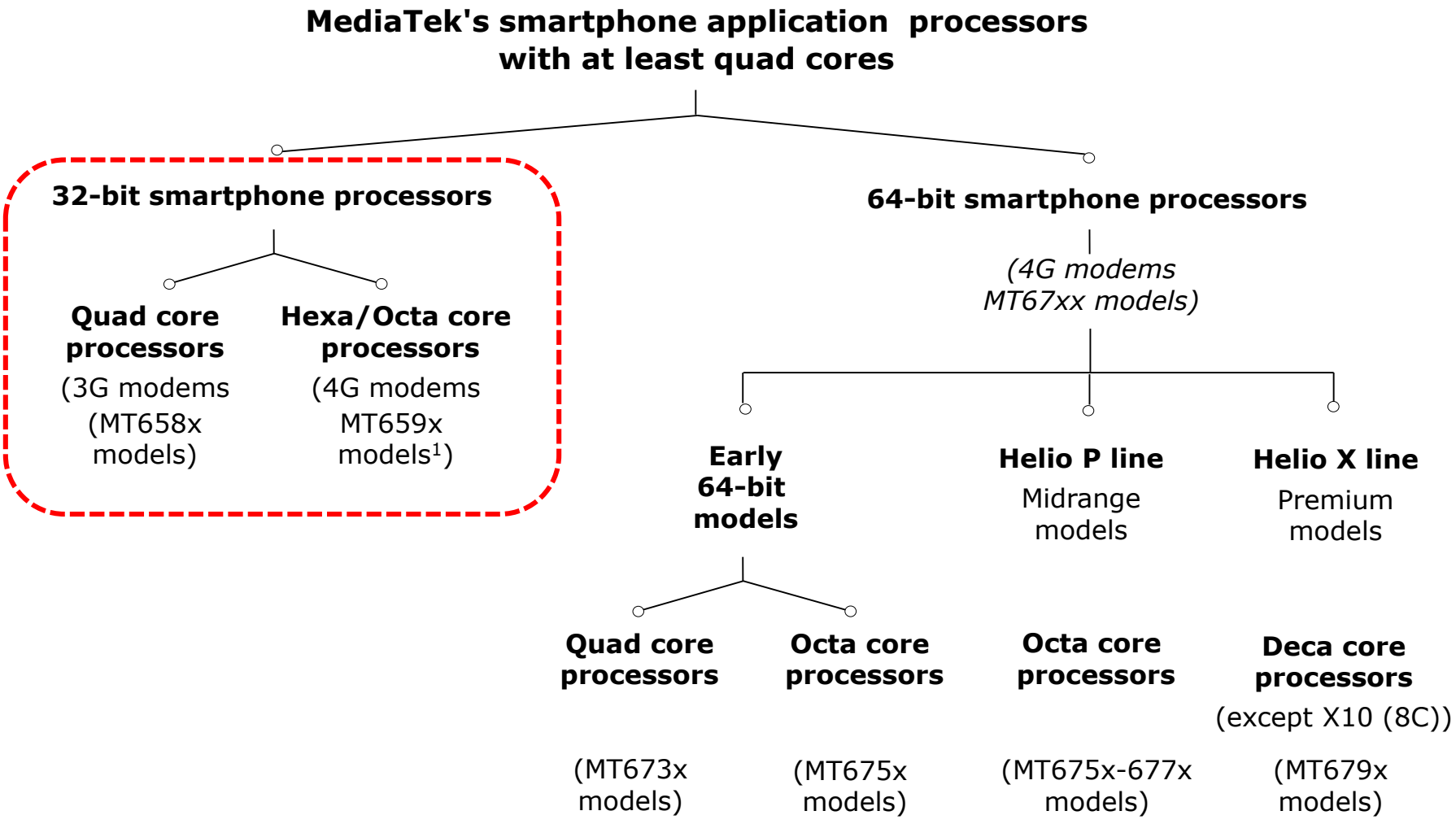
Overview of MediaTek's smartphone processor lines



[1]The MT6591/MT6592 models need an external modem to provide LTE

2.2 MediaTek’s 32-bit smartphone processors

2.2 MediaTek's 32-bit smartphone processors (with at least quad cores)



[1]The MT6591/MT6592 need an external modem to provide LTE

2.2 MediaTek's 32-bit smartphone processors (2)

a) Overview of MediaTek's 32-bit quad core smartphone processors -1 [3]

Model	Intro.	Techn.	Clock speed	CPU cores Cortex -Axx	GPU	GPU clock	Max. Mega Pixel	Max. Resolution	Net work	Used in
MT6582	Q3/2013	28nm	1.3GHz	4x A7	ARM Mali400-MP2	500 MHz	13 MP	720*1280	3G	OPPO R1
MT6582M	07/2013	28nm	1.3GHz	4x A7	ARM Mali400-MP2	416 MHz	8.0 MP	540*960	3G	Lenovo A850
MT6588	Q4/2013	28nm	1.7GHz	4x A7	PowerVR SGX544	600 MHz	13 MP	1280*800	3G	Gionee E6
MT6589	03/2013	28 nm	1.2 GHz	4x A7	PowerVR SGX544	286 MHz	13 MP	1920*1080	3G	Large number of mobiles
MT6589M	07/2013	28nm	1.2GHz	4x A7	PowerVR SGX544	286 MHz	13 MP	1920*1080	3G	Sony Xperia C3
MT6589T	07/2013	28nm	1.5GHz	4x A7	PowerVR SGX544	357 MHz	13 MP	1920*1080	3G	Vivo X3t

Overview of MediaTek's 32-bit quad/octa core smartphone processors -2

- The above Table indicates that all of MediaTek's 32-bit quad core processors are implemented as symmetrical multicore processors.
- Next, as an example we will briefly discuss MediaTek's most widespread used 32-bit quadcore processor, the MT6589.

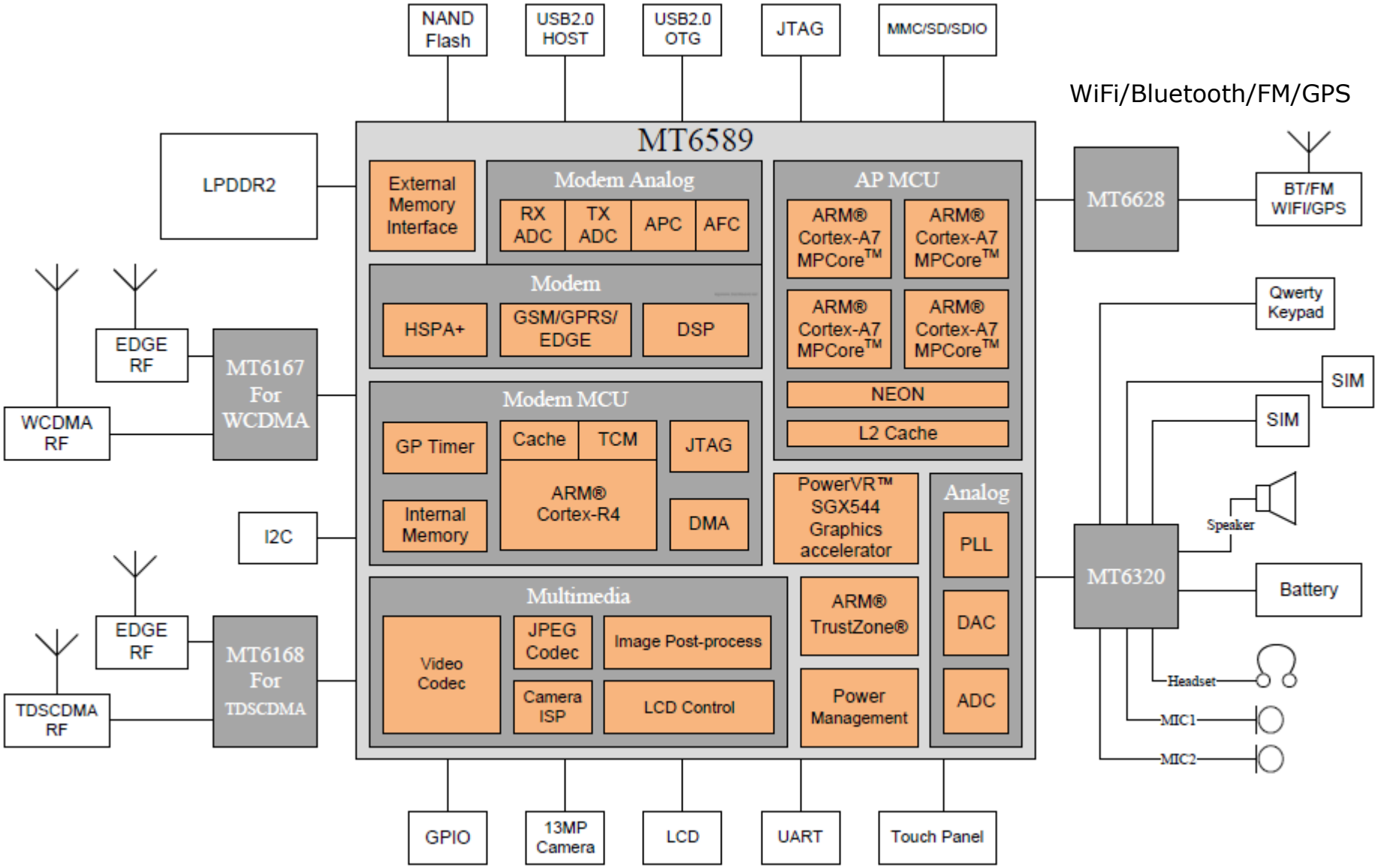
2.2 MediaTek's 32-bit smartphone processors (4)

Example for MediaTek's 32-bit quad core smartphone SOCs built in symmetrical multicore style: The MT6589 (2012)

- The MT6589 was the world's first quad core Cortex-A7 based SOC.
- It includes also an integrated HSPA+ 3G baseband modem.
- The MT6589 is MediaTek's most widespread used SOC incorporated in a large number of cheap smartphones.
- The next Figure shows its block diagram.

2.2 MediaTek's 32-bit smartphone processors (5)

Block diagram of the MT6589 32-bit quad core smartphone processor [4]



2.2 MediaTek’s 32-bit smartphone processors (6)

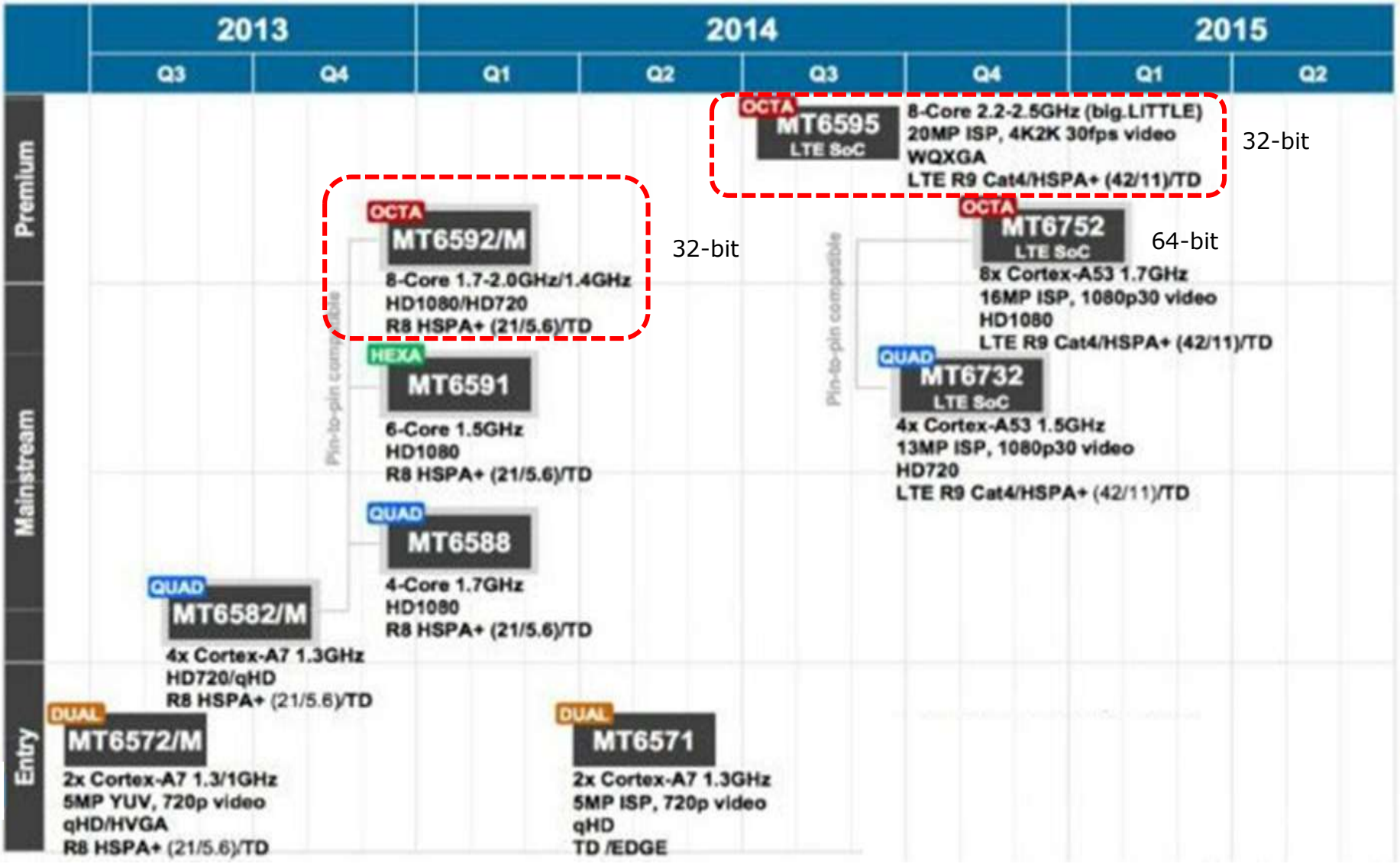
b) Overview of MediaTek's 32-bit octa core smartphone processors [3]

Subsequently we will focus on MediaTek’s 32-bit octa core smartphone application processors.

These processors are high-end designs processors, as indicated in their 2013-2015 roadmap, shown in the next Figure.

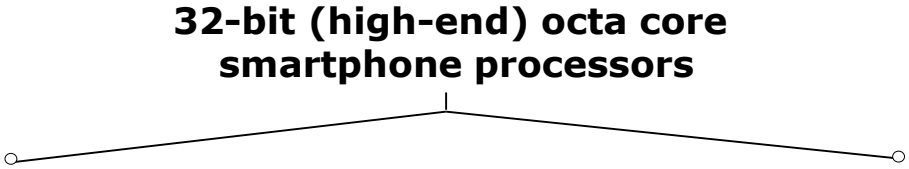
2.2 MediaTek's 32-bit smartphone processors (7)

Introduction of 32-bit octa core smartphone application processors for the high-end market segment [25]



2.2 MediaTek's 32-bit smartphone processors (8)

Overview of MediaTek's 32-bit (high-end) octa core smartphone processors



MT6592 (11/2013)

Built up
as symmetrical multicore
processor

The world's first 32-bit octa core
smartphone processor
operating in symmetrical multicore mode
It supports HSPA+ (4G)

MT6595 *(07/2014)*

Built up
as big.LITTLE multicore processor
with dual clusters

The world's first true 32-bit octa core
smartphone processor
operating in the big.LITTLE mode
and supporting LTE (4G)

True octa cores in case of a big-LITTLE configuration means inclusive core switching (aka GTS (Global Task Scheduling)), allowing all eight cores to operate at the same time.

2.2 MediaTek’s 32-bit smartphone processors (9)

Main features of MediaTek's 32-bit hexa/octa core smartphone processors

	Available	Techn.	Market sector	CPU	fc	GPU	Modem	Task-scheduling
MT6591	4/2014	28 nm	High-end	6x Cortex-A7	1.50 GHz	Mali-450MP	HSPA+ (3G), LTE cat. 4 with an ext. modem[1]	CorePilot
MT6592	11/2013	28 nm	High-end	8x Cortex-A7	2.0 GHz	Mali-450MP	HSPA+ (3G), LTE cat. 4 with an ext. modem[1]	CorePilot
MT6595	7/2014	28 nm	High-end	4x A17+ 4x A7	2.2 GHz	G6200	LTE Cat. 4	CorePilot

[1]The MT6591/MT6592 processors provide LTE cat. 4 connectivity along with the MT6290 external modem.

Example 1: MediaTek's first 32-bit octacore smartphone SOC built in symmetrical multicore style: the MT6592 (2013)

- It is the industry's first 32-bit true octa core mobile processor, meaning that all eight cores may be active at the same time, as indicated below.

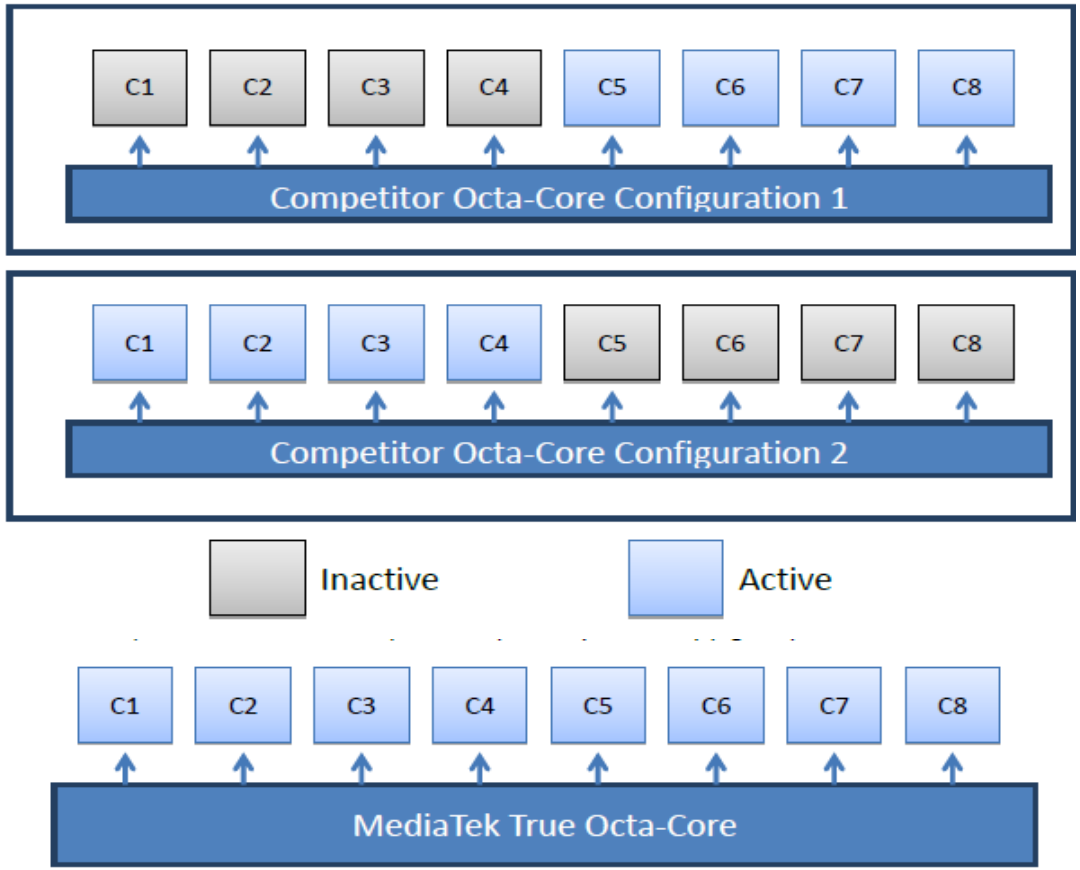


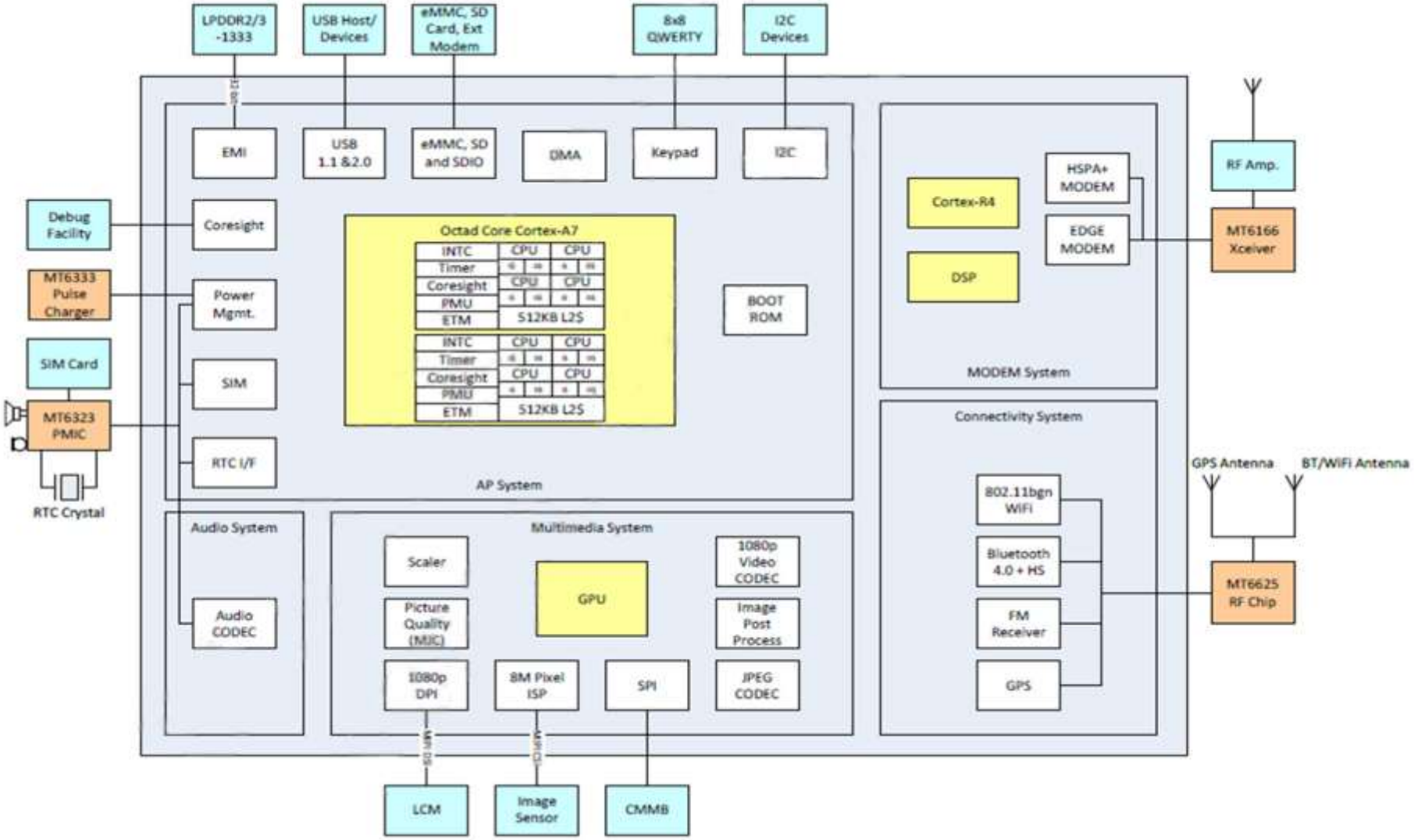
Figure: Operation of MediaTek's true octa core MK6592 supported by Corepilot [5]

Main features of the MT6592-2

	Available	Techn.	Market sector	CPU	fc	GPU	Modem	Task-scheduling
MT6592	11/2013	28 nm	High-end	8x Cortex-A7	2.0 GHz	Mali-450MP	HSPA+	CorePilot

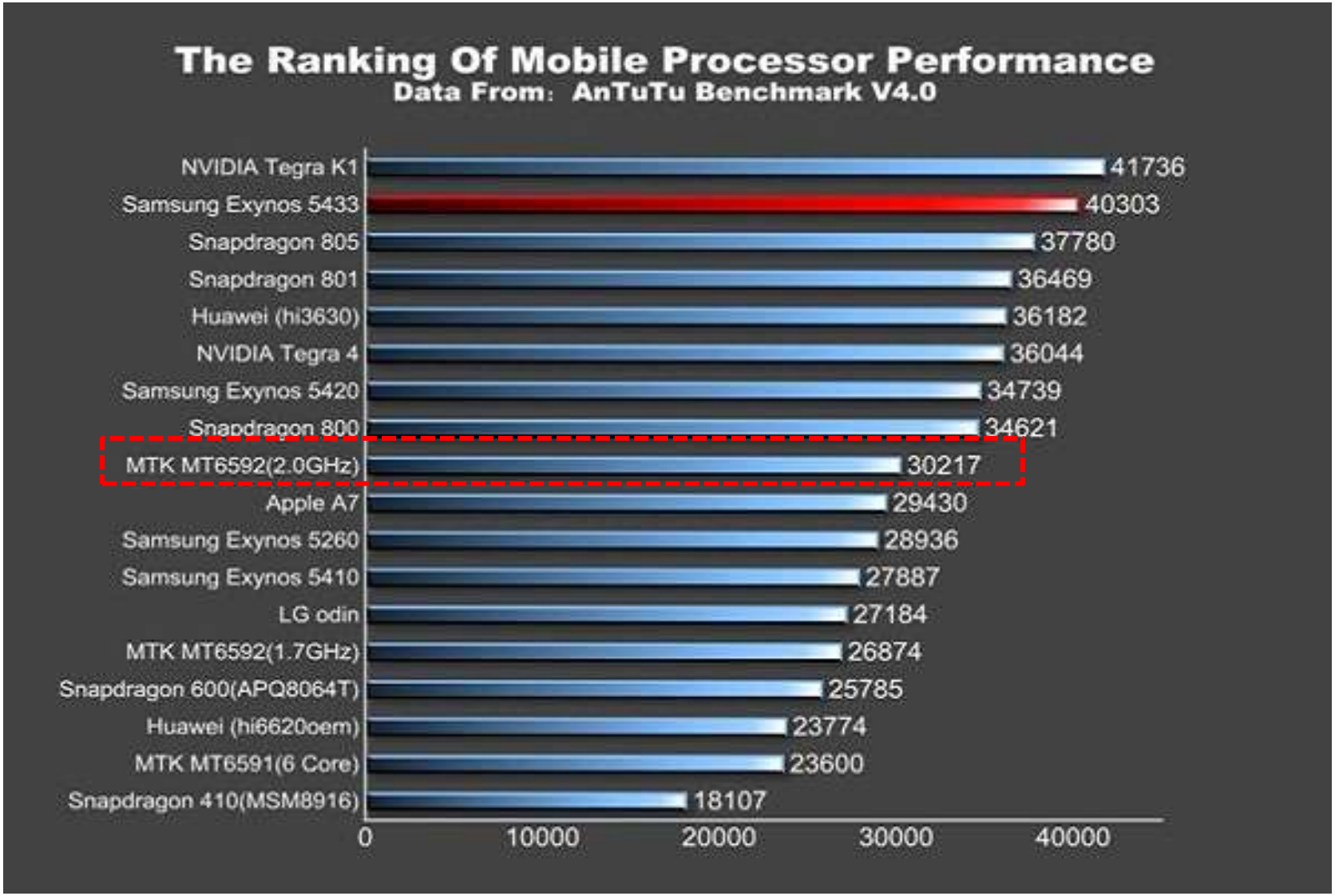
2.2 MediaTek's 32-bit smartphone processors (12)

Block diagram of the 32-bit true octa core MT6592 smartphone processor built up as a symmetrical multicore [6]



2.2 MediaTek's 32-bit smartphone processors (13)

The performance of the MT6592 vs. other mobile processors [7]



Example 2: MediaTek's first true 32-bit octa core smartphone SOC built in big.LITTLE style: the MT6595 (2014)

- It is the world's first 32-bit true octa core smartphone SOC in big.LITTLE configuration.
- It is MediaTek's solely 32-bit smartphone processor built in big.LITTLE style.
- Announced in 2/2014, at the same time when ARM introduced the Cortex-A17, with samples for OEMs shortly thereafter.
- Available in 09/2014 is smartphones (Meizu MX4).
- The MT6595 supports LTE.
- All eight cores may be active at the same time, i.e. the MT6595 implements inclusive core switching, called also GlobalTask Scheduling (GTS).

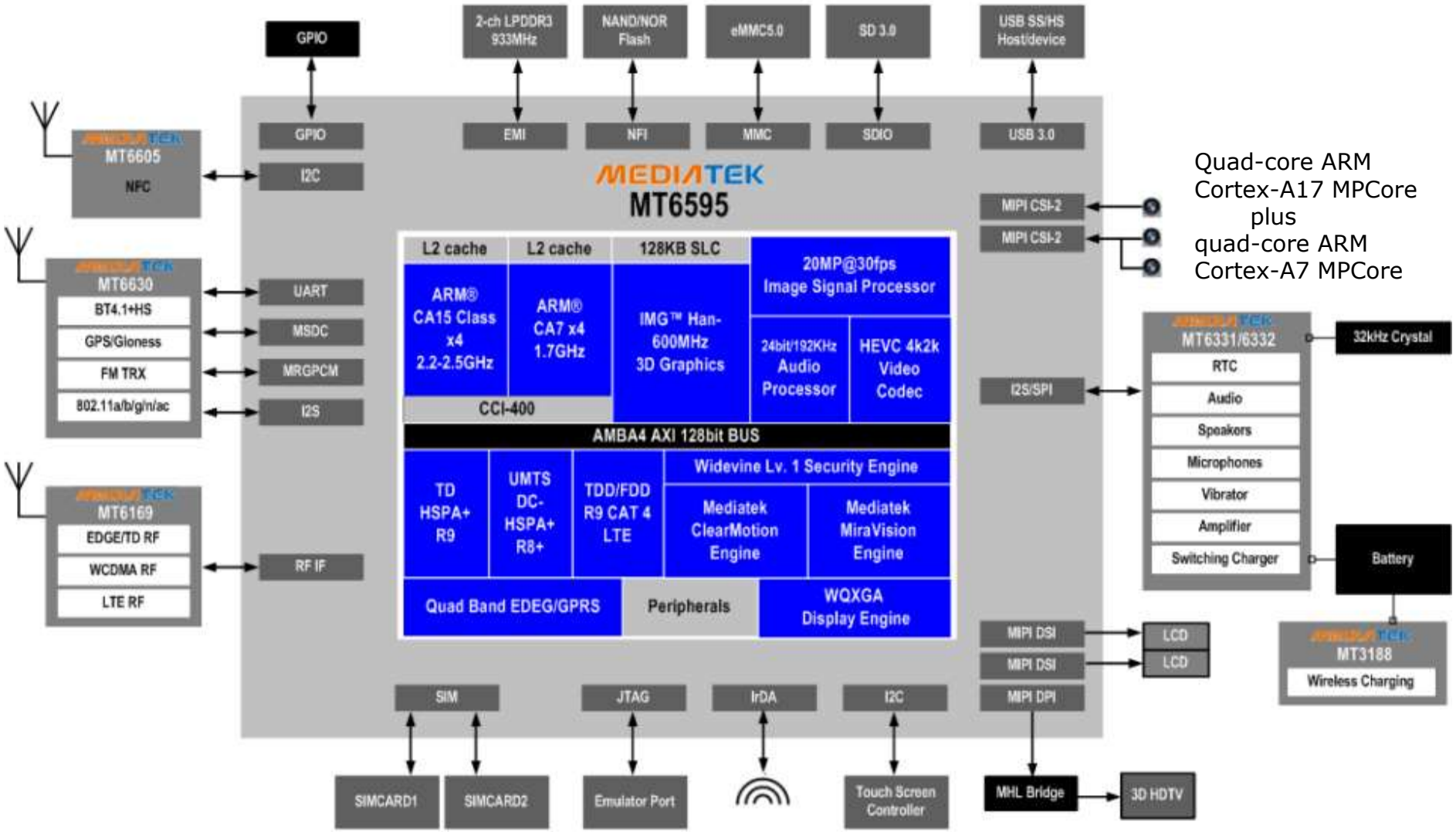
2.2 MediaTek's 32-bit smartphone processors (15)

Key features of MediaTek's 32-bit true octa core smartphone SOC built in big.LITTLE multicore style

	Available	Techn.	Market sector	CPU	fc	GPU	Modem	Task-scheduling
MT6595	7/2014	28 nm	High-end	4x A17+ 4x A7	2.2 GHz	G6200	LTE Cat. 4	CorePilot

Block diagram of MT6595 Octa core big.LITTLE LTE platform [8]

Corepilot



2.2 MediaTek's 32-bit smartphone processors (17)

Remark

Related to many SOC models MediaTek has three model version, as follows

- the basic version, without any tag
- the model version tagged by M and
- the model version taged by T.:

Interpretation of the M and T model versions

M: means Middle Class, it has lower performance paramenters than the base version

T: means Turbo, it has higher performance parameters than the base version

As an example below we show main parameters of the MT6595 and MT6595M model versions.

Contrasting main features of the octa core big.LITTLE MT6595M/MT6595 SOCs [9]

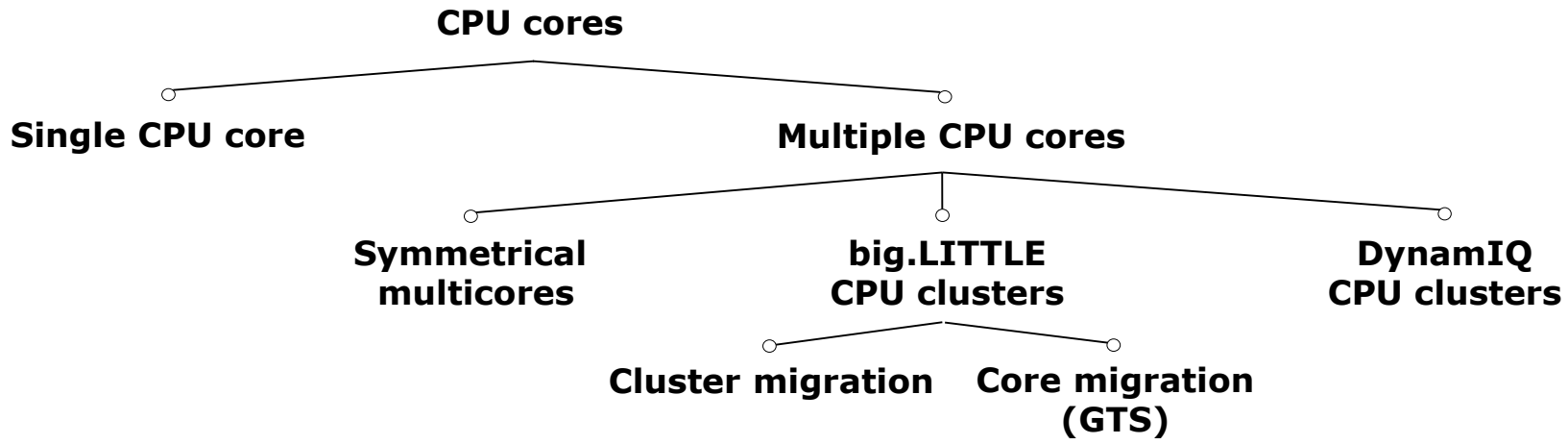
- 5 -	MT6595M	MT6595
Process	28nm HPM	28nm HPM
Apps CPU	Big Core: 2GHz Little Core: 1.5GHz 32KB/32KB L1, 2MB L2	Big Core: 2.1-2.2GHz Little Core: 1.7GHz 32KB/32KB L1, 2MB L2
Memory	2x LPDDR3 933MHz PoP	2x LPDDR3 933MHz PoP
Camera	16MP ISP	20MP ISP
Video Decode	4Kx2K 30fps H.265/H.264	4Kx2K 30fps H.265/H.264
Video Encode	FHD 60fps H.265/H.264	4Kx2K 30fps H.265
Graphics	IMG Rogue G6200 450MHz	IMG Rogue G6200 600MHz
Display	FHD 1920x1080	WQXGA 2560x1600
Modem	LTE FDD/TDD R9 Cat4 DC-HSPA+ 42/11Mbps TD-SCDMA/EDGE	LTE FDD/TDD R9 Cat4 DC-HSPA+ 42/11Mbps TD-SCDMA/EDGE
Connectivity	External MT6630 Wi-Fi 11ac/abgn/BT/FM/GPS	External MT6630 Wi-Fi 11ac/abgn/BT/FM/GPS

2.2 MediaTek's 32-bit smartphone processors (19)

Remark to the true octa operation of the MT6595 built in the big.LITTLE style

- Running under the CorePilot software the four high-performance ARM Cortex-A17 and the four low power Cortex-A7 cores may be activated in any combination.
- This provides alltogether high performance by low power consumption.

Evolution of the CPU architecture in MediaTek's mobiles



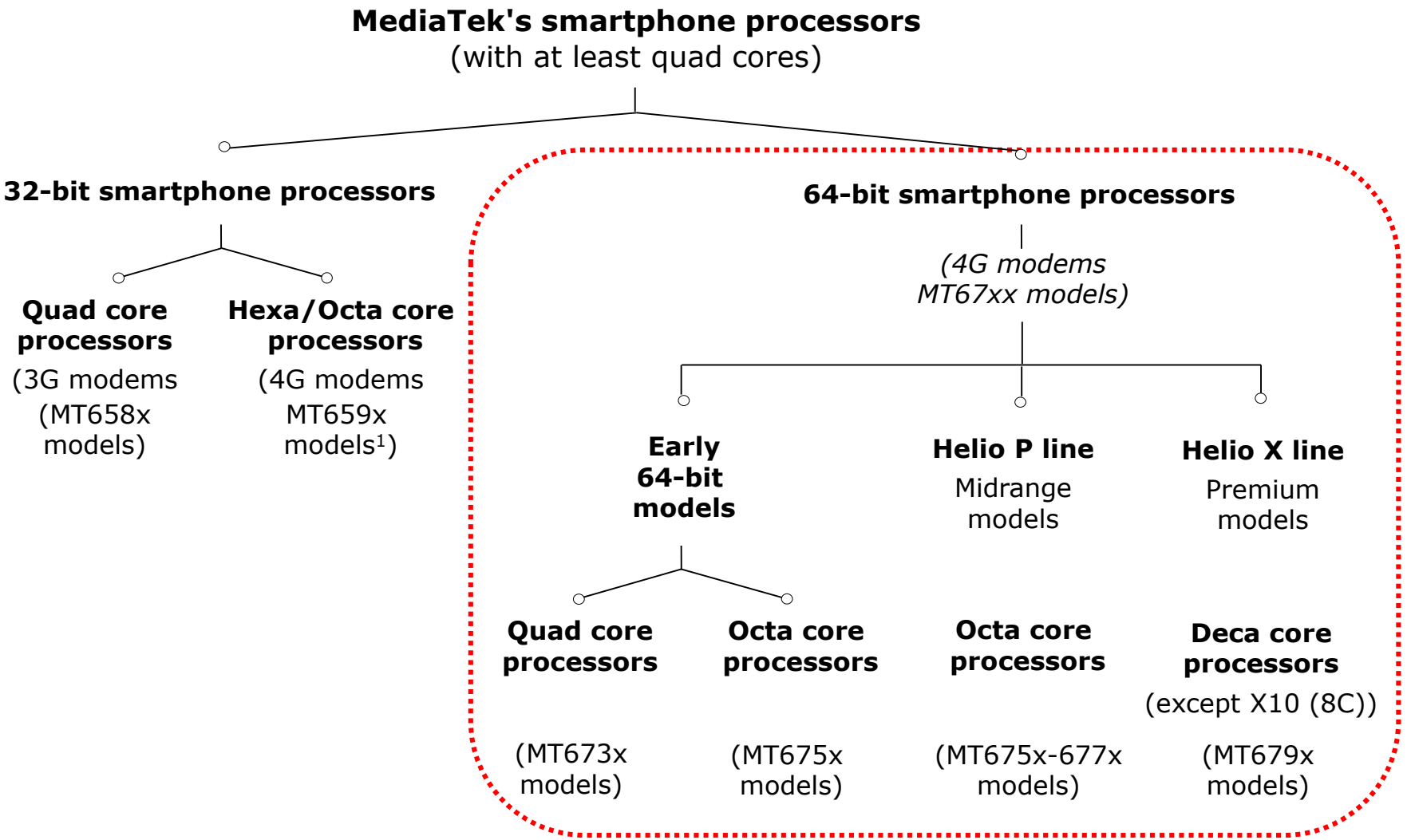
Apple	*ARM1176 (2007) until A4 (2010)* →	*A5 (2011) (2C)* →	*A10 (2016) (2+2)* →	*A11 (2017) (2+4)*	
Samsung Exynos	*3110 (2010)* →	*3250 2C (2011) 4412 4C (2012)* →	*5410 (2013) (4+4)* →	*5420 (2013) (4+4)* →	*9810 (2018) (4+4)*
Qualcomm Snapdragon	*MSM 7225 (2010)* →	*8260 2C (2013) 400 4C (2013)* →		*808 (2+4) (2014) 810 (4+4) (2015)* →	*845 (2018) (4+4)*
Huawei Kirin	*(K3V1) (2009)* →	*(K3V2 (2012))* →		*920 (4+4)) 2014)* →	*980 (2018) (4+4)*
MediaTek	*MT6218B (2003)* →	*MT6582 4C (2013) MT6592 8C (2013)* →		*MT6595 8C (2014)* →	*MT6795 10C (2019)*

2.3 MediaTek’s 64-bit smartphone processors

- 2.3.1 Overview of MediaTek’s 64-bit smartphone processors
- 2.3.2 MediaTek’s early 64-bit smartphone processors
- 2.3.3 MediaTek’s Helio P midrange line
- 2.3.3 MediaTek’s Helio X high-end line

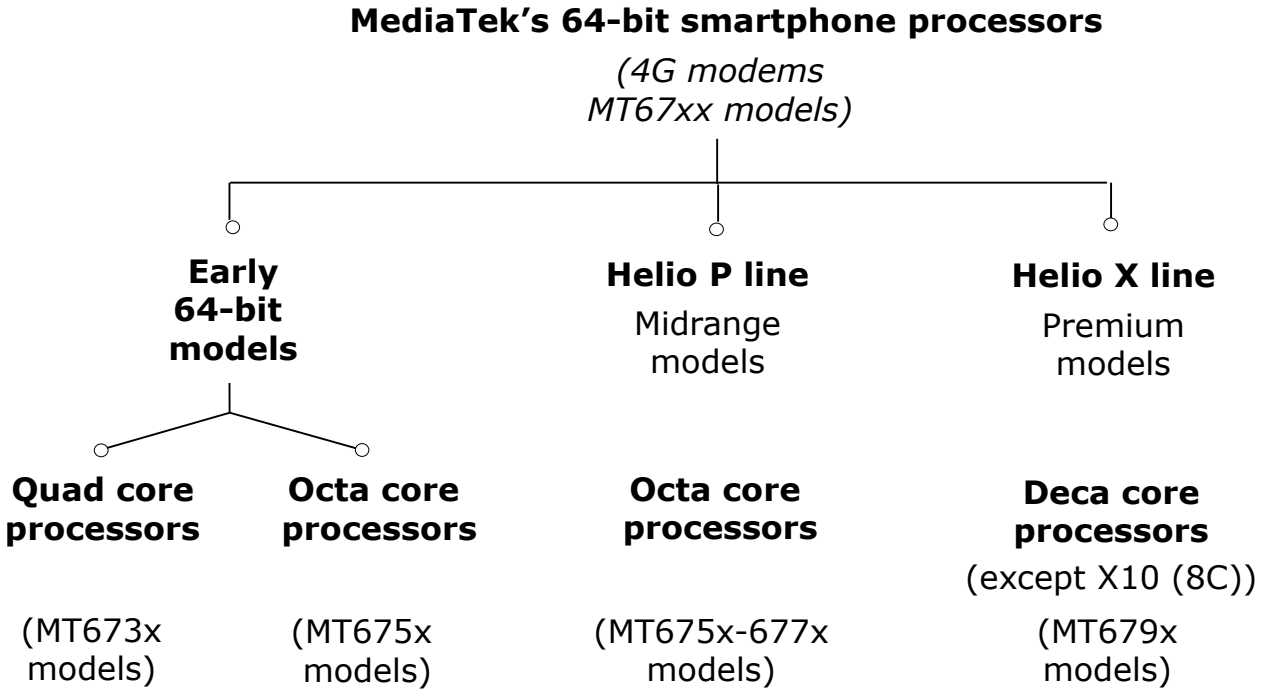
2.3.1 Overview of MediaTek’s 64-bit smartphone processors

2.3.1 Overview of MediaTek's 64-bit smartphone processors



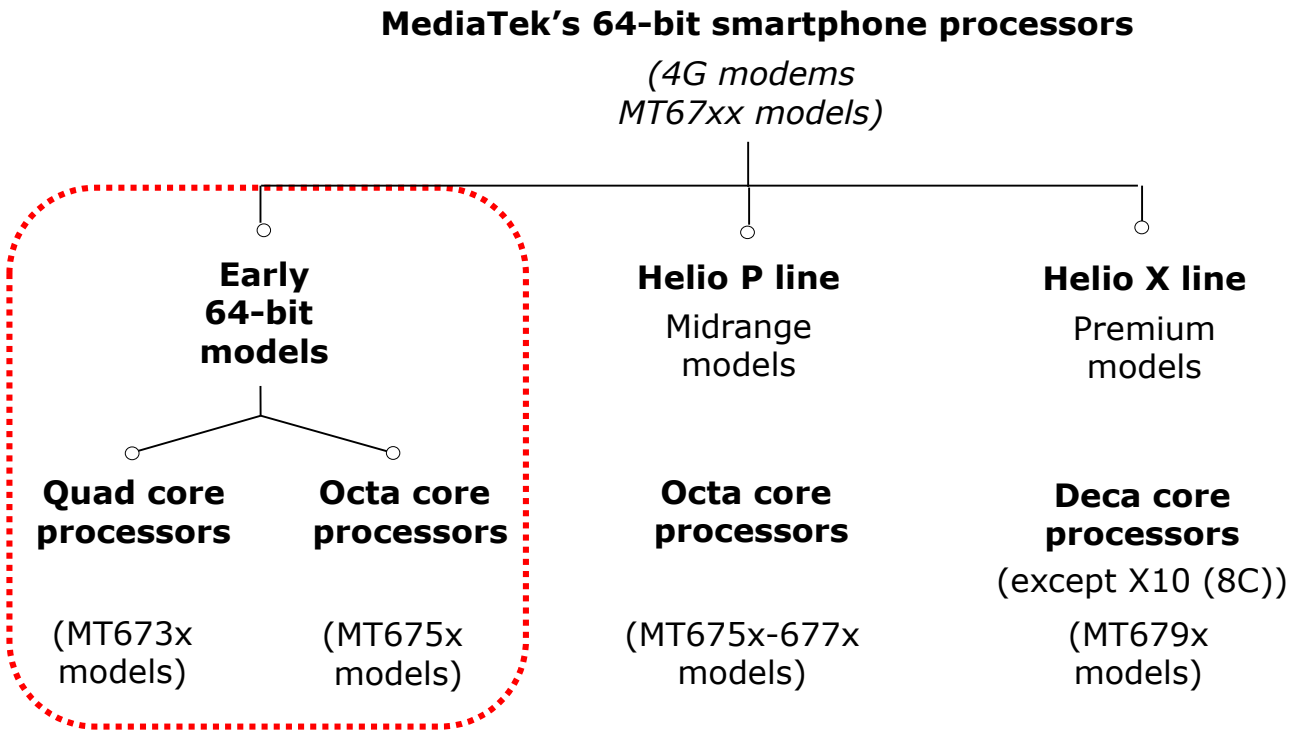
[1]The MT6591/MT6592 need an external modem to provide LTE

Overview of MediaTek's 64-bit smartphone processors



2.3.2 MediaTek’s early 64-bit smartphone processors

2.3.2 MediaTek’s early 64-bit smartphone processors



2.3.2 MediaTek’s early 64-bit smartphone processors (2)

Key features of MediaTek's early 64-bit smartphone processors [3]

Model	Intro.	Techn.	Clock speed	CPU cores Cortex-Axx	GPU	Max. Mega Pixel	Max Resolution	Net work	Used in
MT6732	Q3/2014	28nm	1.5GHz	4x A53	Mali-T760	13 MP	1280*720	4G	Lenovo P70t
MT6735	Q2/2015	28nm	1.3-1.5GHz	4x A53	Mali-T720	13 MP	720*1280	4G	Gionee M3
MT6735M	Q2/2015	28nm	1.0GHz	4x A53	Mali-T720	8 MP	960*540	4G	--
MT6735P	Q2/2015	28nm	1.0GHz	4x A53	Mali-T720	8 MP	720*1280	4G	Elephone S2 Plus
MT6737	Q2/2016	28nm	1.1-1.3GHz	4x A53	Mali-T720	na.	720px1080	4G	DOOGEE X5 Max Pro
MT6737T	Q2/2016	28 nm	1.5GHz	4x A53	Mali-T720	na.	1920x1080	4G	DOOGEE X5 Max Pro
MT6738	Q1/2016	28nm	1.5GHz	4x A53	Mali-T860	13 MP	720*1280	4G	--
MT6752	Q3/2014	28nm	1.7-2.0GHz	8x A53	Mali-T760	16 MP	1920*1080	4G	HTC Desire 616w
MT6795 (Helio X10)	Q4/2015	28nm	2.2GHz	8x A53	PowerVR G6200	20 MP	2560*1600	4G	Elephone Vowney
MT6753	Q3/2015	28nm	1.3-1.5GHz	8x A53	Mali-T720	16 MP	1920*1080	4G	HTC WF5w
MT6750	Q2/2016	28nm	1.5GHz	8x A53	Mali-T860	16 MP	720*1280	4G	--
MT6750T	Q2/2016	28nm	1.5GHz	8x A53	Mali-T860	16 MP	1920*1080	4G	--
MT6755	Q4/2015	28nm	2.0GHz	8x A53	Mali-T860	21MP single or 16MP + 8MP dual	1920*1080	4G	Elephone P9000
MT6755M	Q4/2015	28nm	1.8GHz	8x A53	Mali-T860	16 MP	1920*1080	4G	--

2.3.2 MediaTek's early 64-bit smartphone processors (3)

Note that all early 64-bit quad or octa core processors are symmetrical multicores built up of four or eight A53 cores.

2.3.2 MediaTek’s early 64-bit smartphone processors (4)

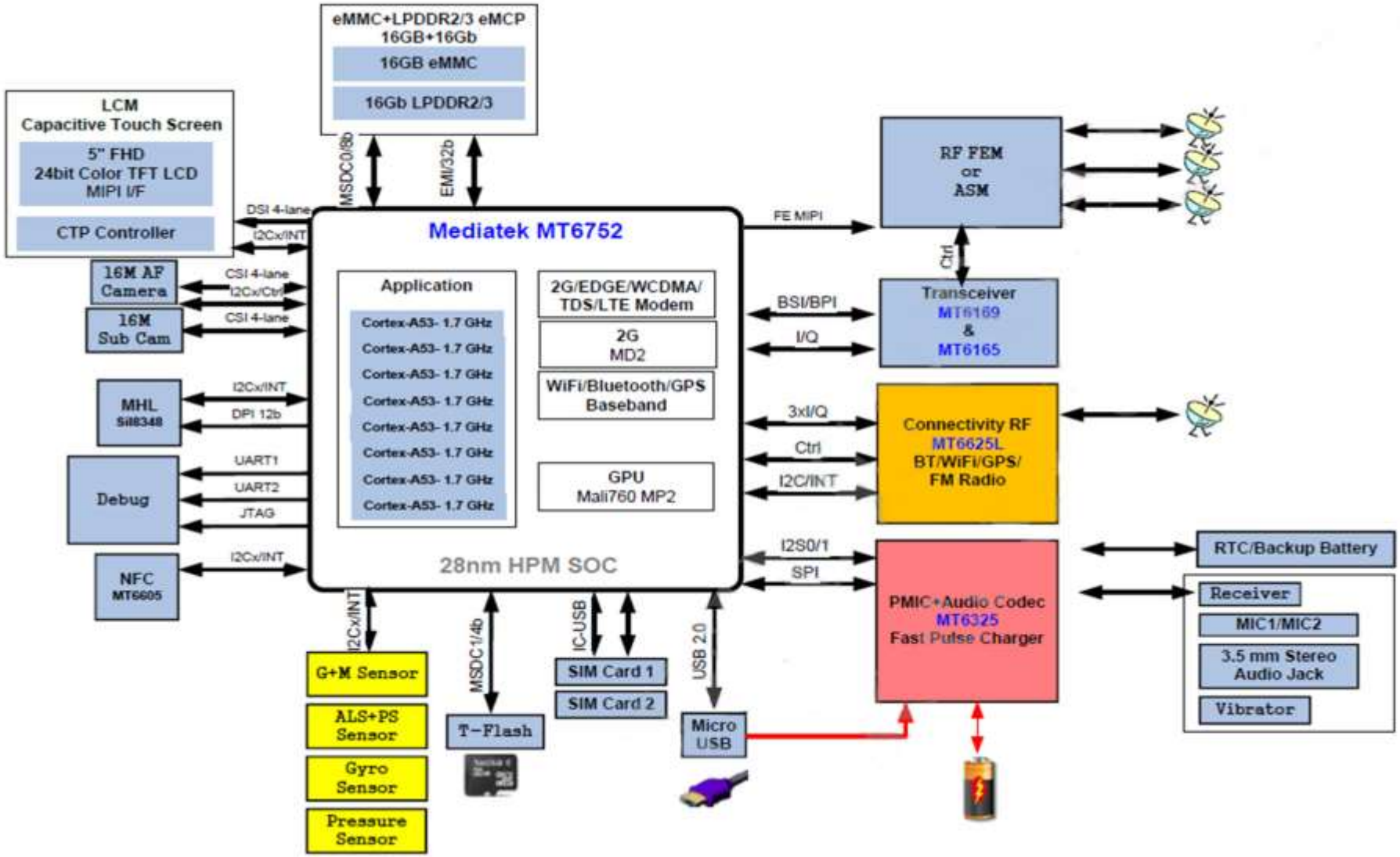
Example for MediaTek's early 64-bit octa core processors: MediaTek’s first 64-bit octa core processor, the MT6752 (2014)

Key parameters of the MT6752 [3]

Model	Intro.	Techn.	Clock speed	CPU cores Cortex-Axx	GPU	Max Mega Pixel	Max Resolution	Net work	Used in
MT6752	Q3/2014	28nm	1.7-2.0GHz	8x A53	Mali-T760	16 MP	1920*1080	4G	HTC Desire 616w

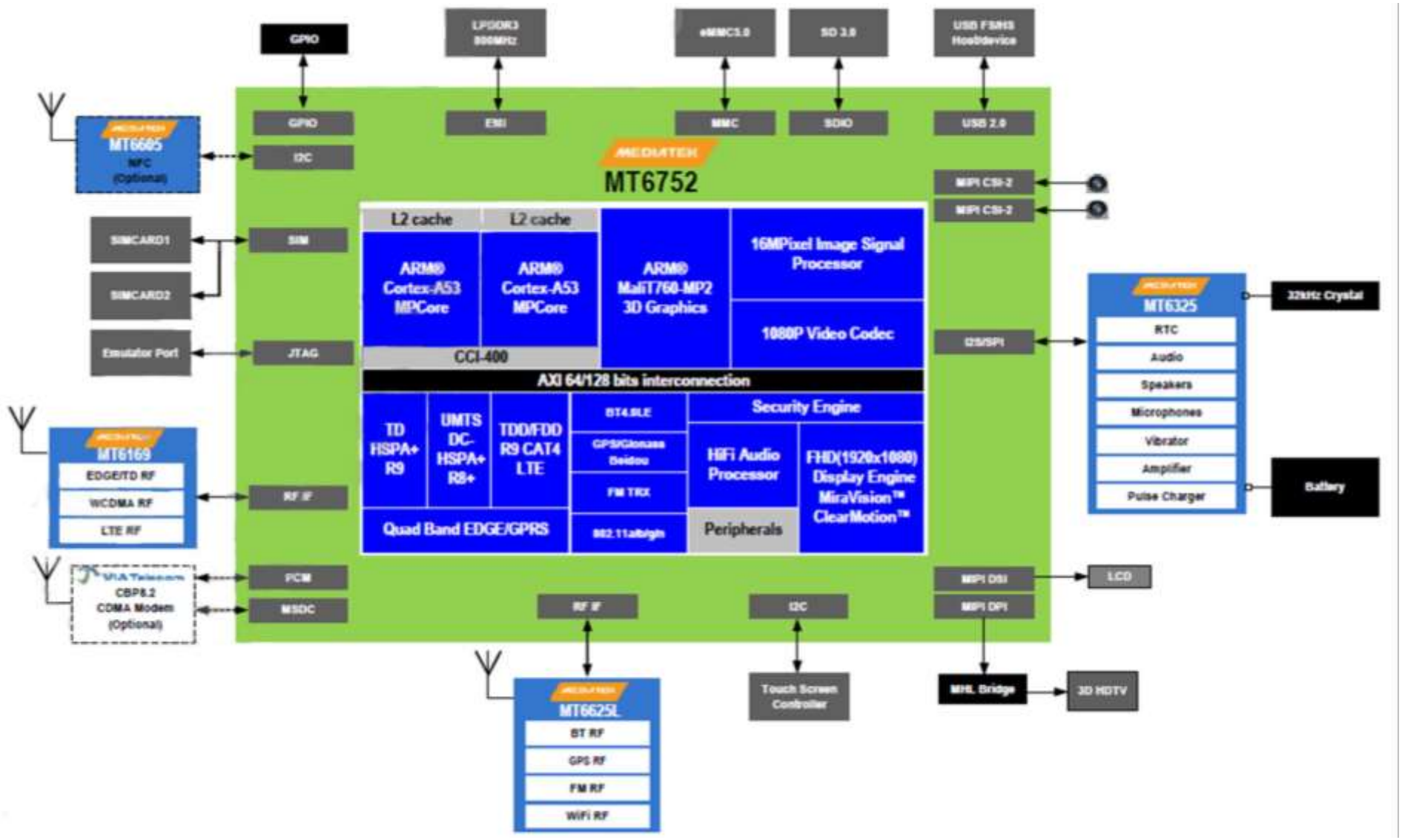
2.3.2 MediaTek's early 64-bit smartphone processors (5)

System level block diagram of the 64-bit octa core MT6752 built up as a symmetrical multicore [10]



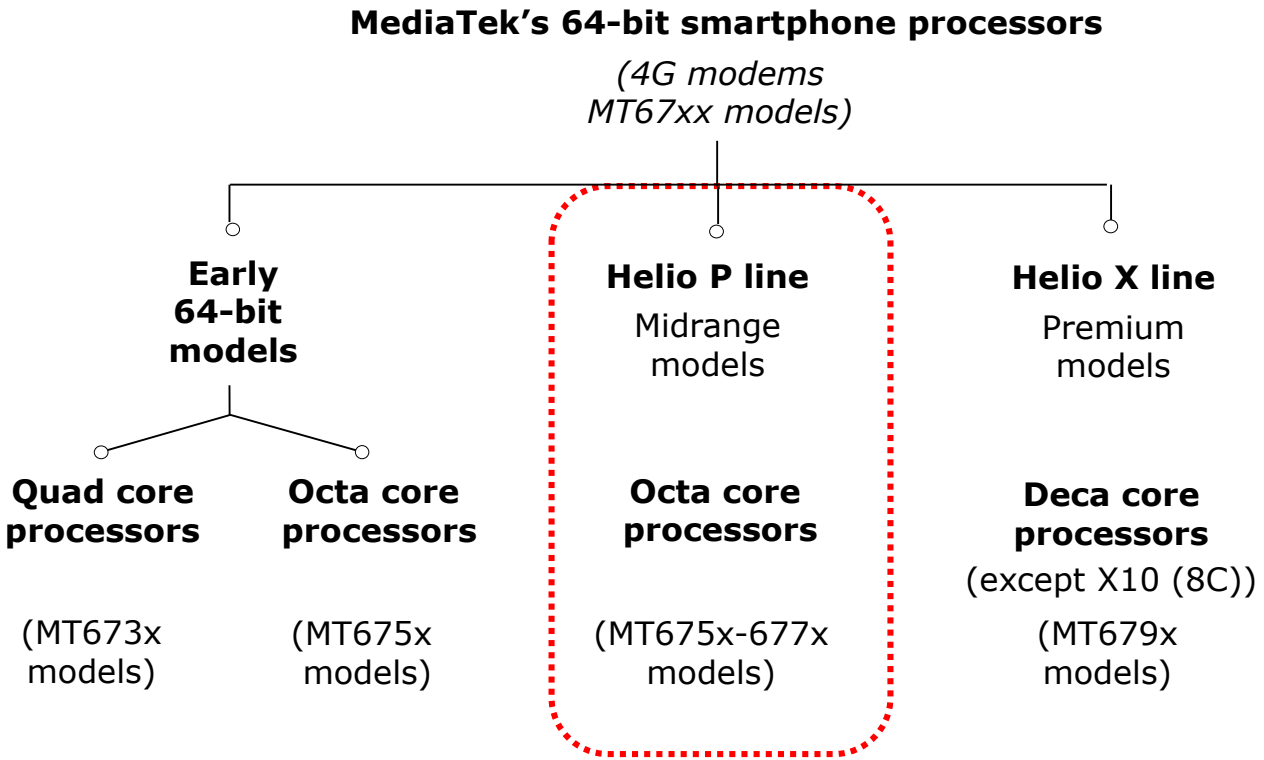
2.3.2 MediaTek's early 64-bit smartphone processors (6)

Block diagram of the 64-bit octa core MT6752 built up as a symmetrical multicore [10]



2.3.3 MediaTek’s Helio P midrange line

2.3.3 MediaTek’s Helio P midrange line



2.3.3 MediaTek's Helio P midrange line (2)

Mediatek's Helio family of smartphone processors

- Launched in 3/2015.
- The Helio family is set up of two lines:
  - the Helio P midrange line
    (nevertheless called as premium performance sub-family by Mediatek) and
  - the Helio X high-end line

as indicated below with boosted designations.

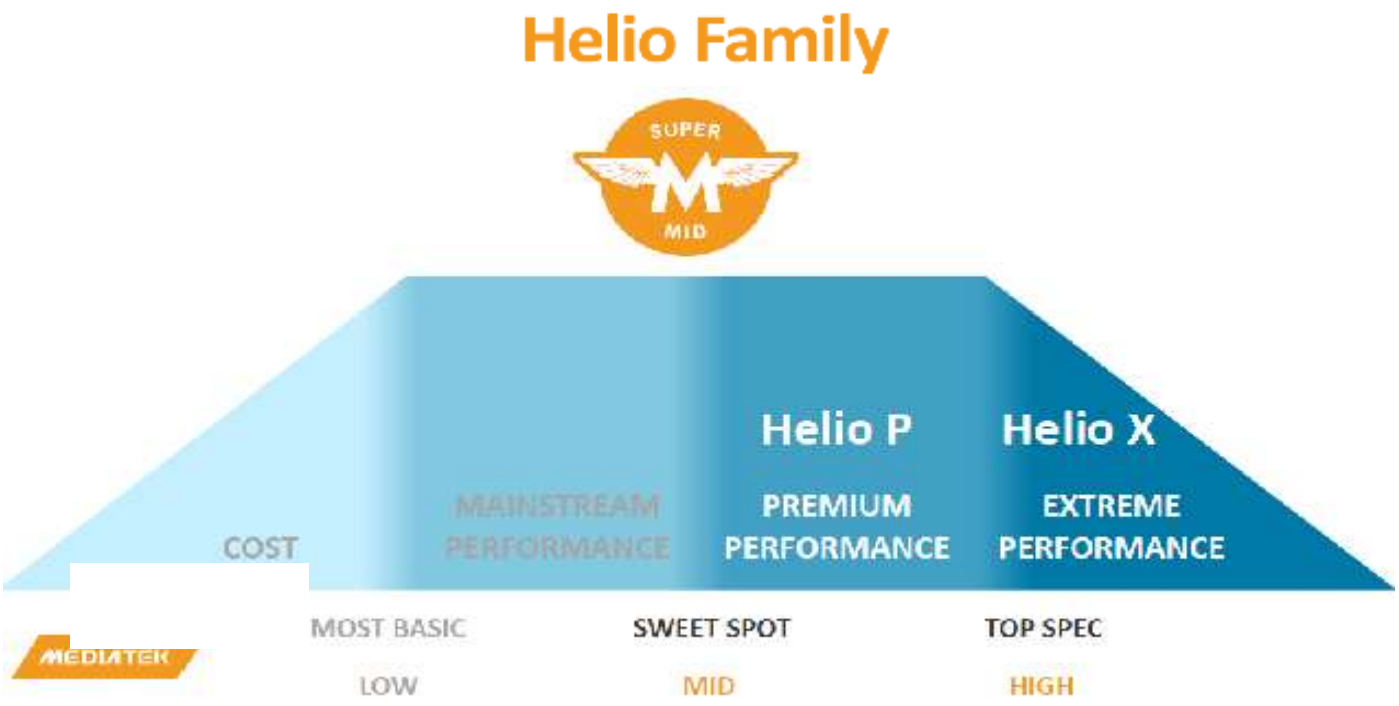


Figure: Sub-families of the Helio family [26]

2.3.3 MediaTek's Helio P midrange line (3)

Main features of MediaTek's midrange Helio P models [3] -1

Model	Launched	Techn.	Configura-tion	GPU	Memory (POP)	Connect. up to	CorePilot version
Helio P10 (MT6755)	06/2015	28 nm	4xA53 2.0 GHz+ 4xA53 1.2 GHz	Mali T860 MP2 700 MHz	1xLPDDR3 933 Mbps	LTE cat. 6	CorePilot (2.0)
Helio P15 (MT6755T)	Q3/2016	28 nm	4xA53 2.2 GHz+ 4xA53 1.2 GHz	Mali T860 MP2 700 MHz	1xLPDDR3 933 Mbps	LTE cat. 6	CorePilot (2.0)
Helio P18 (MT6755S)	Q1/2018	28 nm	8xA53 2.0 GHz	Mali T860 MP2 800 MHz	1xLPDDR3 933 Mbps	LTE cat. 6	CorePilot (4.0)
Helio P20 (MT6757)	Q3/2016	16 nm	4xA53 2.3 GHz 4xA53 1.6 GHz	Mali T880 MP2 900 MHz	2xLPDDR4x (16-bit) 1600 Mbps	LTE cat. 6	CorePilot (2.0)
Helio P23 (MT6763)	Q3/2017	16 nm	8xA53 2.3 GHz	Mali G71 MP2 770 MHz	2xLPDDR4x (16-bit) 1600 Mbps	LTE cat. 7/13	CorePilot (4.0)
Helio P25 (MT6757T)	Q1/2017	16 nm	4xA53 2.6 GHz 4xA53 1.6 GHz	Mali T880 MP2 100 MHz	2xLPDDR4x 1600 Mbps	LTE cat. 6	CorePilot (2.0)
Helio P30 (MT6758)	Q3/2016	16 nm	4x A53 2.3 GHz 4x A53 1.65 GHz	Mali-G71 MP2 950 MHz	2xLPDDR4x 1600 Mbps	LTE cat. 6	CorePilot (2.0)

2.3.3 MediaTek’s Helio P midrange line (4)

Main features of MediaTek's midrange Helio P models [3] -2

Model	Launched	Techn.	Configura-tion	GPU	Memory (POP)	Connect. up to	CorePilot version
Helio P22 (MT6763T)	Q2/2019	12 nm	8x A53 2.0 GHz	IMG PowerVR GE8320 650 MHz	1xLPDDR4x 16 1600 Mbps	LTE cat. 7/13	CorePilot (4.0)
Helio P35 (MT6765)	Q1/2019	12 nm	8x A53 2.3 GHz	PowerVR GE8320 680MHz	2xLPDDR4x 16 1600 Mbps	LTE cat. 7/13	CorePilot (4.0)
Helio P60 (MT6771)	Q1/2018	12 nm	4xA73 2.0 GHz+ 4xA53 2.0 GHz	Mali G72 MP3 800 MHz	2xLPDDR4x 1800 Mbps	LTE cat. 6/13	CorePilot (4.0)
Helio P70 (MT6771T)	Q4/2018	12 nm	4xA73 2.1 GHz+ 4xA53 2.0 GHz	Mali G72 MP3 900 MHz	2xLPDDR4x 1800 Mbps	LTE cat. 7/13	CorePilot (4.0)
Helio P90 (MT6779)	Q1/2019	12 nm	2xA75 2.2 GHz+ 6xA55 2.0 GHz	PowerVR GM9446 970MHz	2xLPDDR4x 1866 Mbps	LTE cat. 12/13	CorePilot (4.0)

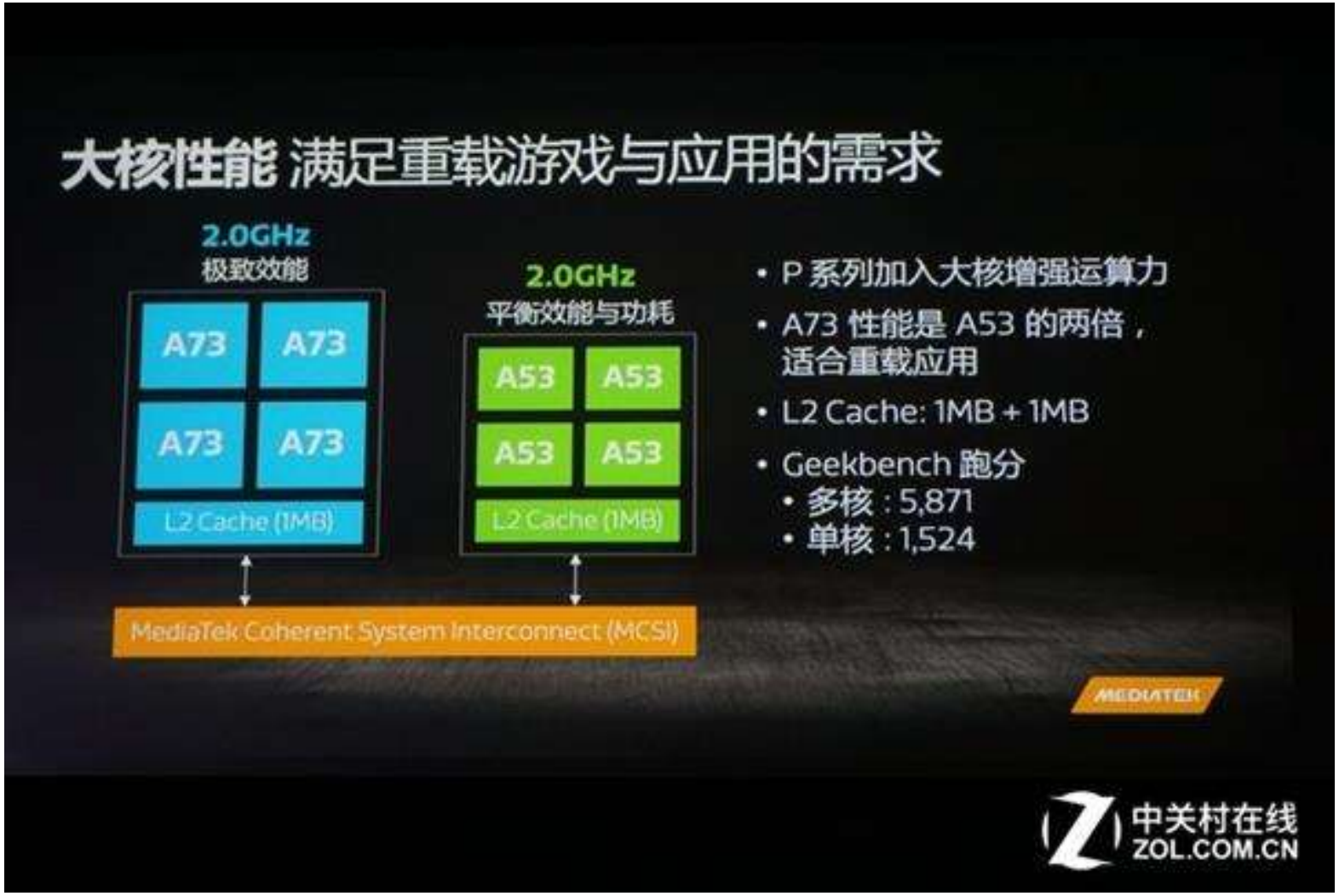
2.3.3 MediaTek’s Helio P midrange line (5)

Example 1: The Helio P60 midrange model

- It is MediaTek’s firs 12 nm model, launched in 03/2018.
- It is also MediaTek’s first processor including a dedicated AI unit, called APU (AI Processing Unit).

2.3.3 MediaTek's Helio P midrange line (6)

Simplified block diagram of the P60 midrange model [30]



2.3.3 MediaTek's Helio P midrange line (7)

Main features of Mediatek's Helio P60 midrange model [31]

MediaTek Current P-Series			
SoC	**Helio P23**	**Helio P30**	**Helio P60**
CPU	4x Cortex A53 @ 2.3GHz 4x Cortex A53 @ 1.65GHz	4x Cortex A53 @ 2.3GHz 4x Cortex A53 @ 1.65GHz	4x Cortex A73 @ 2.0GHz 4x Cortex A53 @ 2.0GHz
GPU	Mali G71MP2 @ 770MHz	Mali G71MP2 @ 900MHz	Mali G72MP3 @ 800MHz
APU / NPU / AI Proc. / Neural IP	-		2x 140GMACs
Memory	1x 32bit LPDDR3 @ 933MHz 2x 16bit LPDDR4X @1500MHz	2x 16bit LPDDR4X @ 1600MHz	1x 32bit LPDDR3 @ 933MHz 2x 16bit LPDDR4X @ 1800MHz
ISP/Camera	1x 24MP or 2x 13MP	1x 25 MP or 2x 16MP	1x 32MP or 2x 20+16MP
Encode/ Decode	2160p30 H.264	2160p30 H.264 & HEVC	2160p30 H.264 & HEVC
Integrated Modem	Category 6 DL = 300Mbps 3x20MHz CA, 64-QAM UL = 50Mbps 64-QAM	Category 7/13 DL = 300Mbps 3x20MHz CA, 64-QAM UL = 150Mbps 2x20MHz CA,64-QAM	Category 7/13 DL = 300Mbps 3x20MHz CA, 64-QAM UL = 150Mbps 2x20MHz CA,64-QAM
Mfc. Process	16FFC	16FFC	12FFC

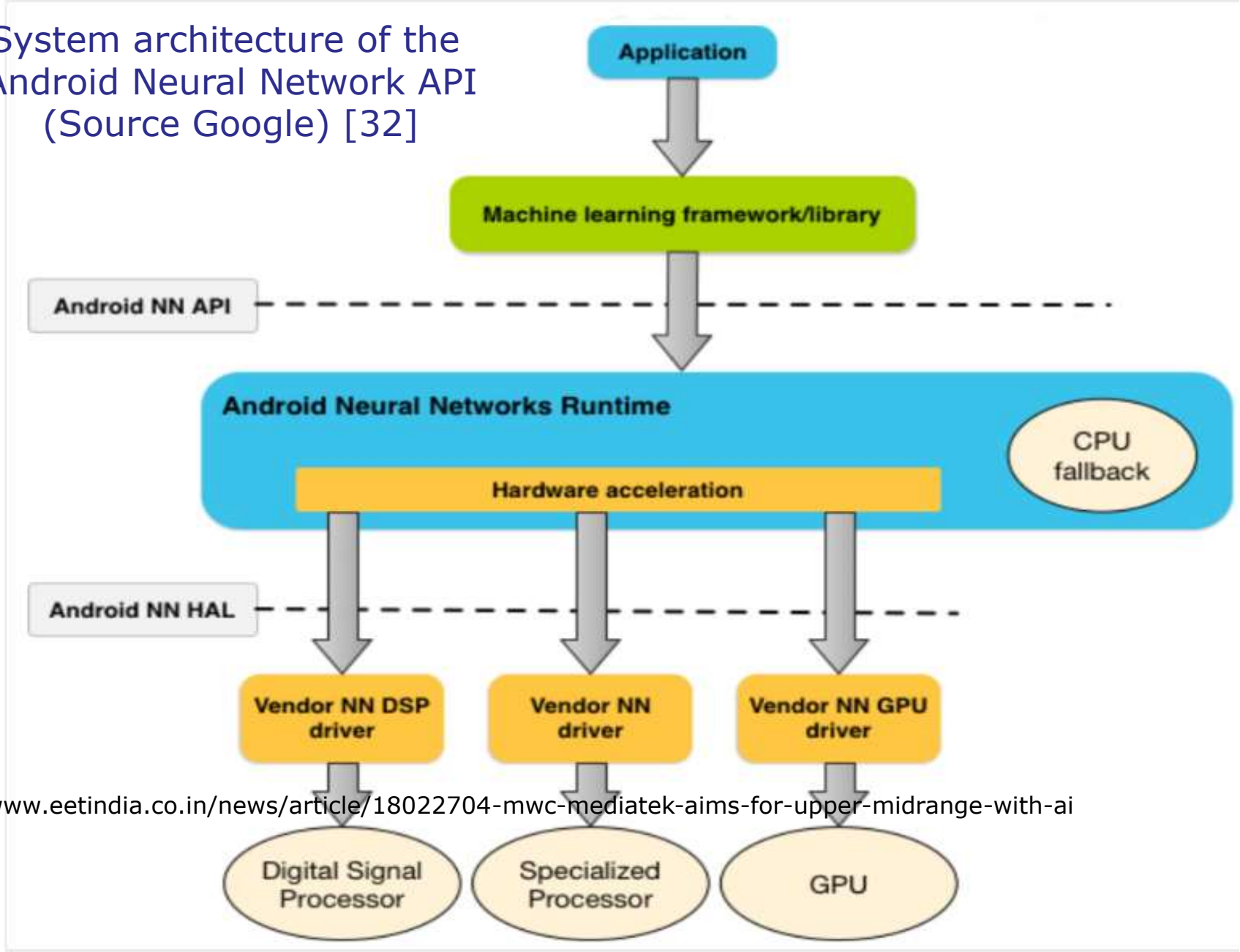
2.3.3 MediaTek's Helio P midrange line (8)

Introduction of AI Processing Units (APUs) into the Helio P line

- MediaTek's first processor with a dedicated neural network accelerator (called APU) was the Helios P60, launched in 03/2018.
- The APU is a dual-core implementation of the Tensilica Vision P6 DSP, featuring 2x140 GMAC/s (multiply-accumulate operations per sec.).
- The available software stack is called NeuroPilot.
- It is compatible with Google's NN API and supports AI frameworks, such as the TensorFlow, TF Lite, Caffe and Caffe2.

2.3.3 MediaTek's Helio P midrange line (9)

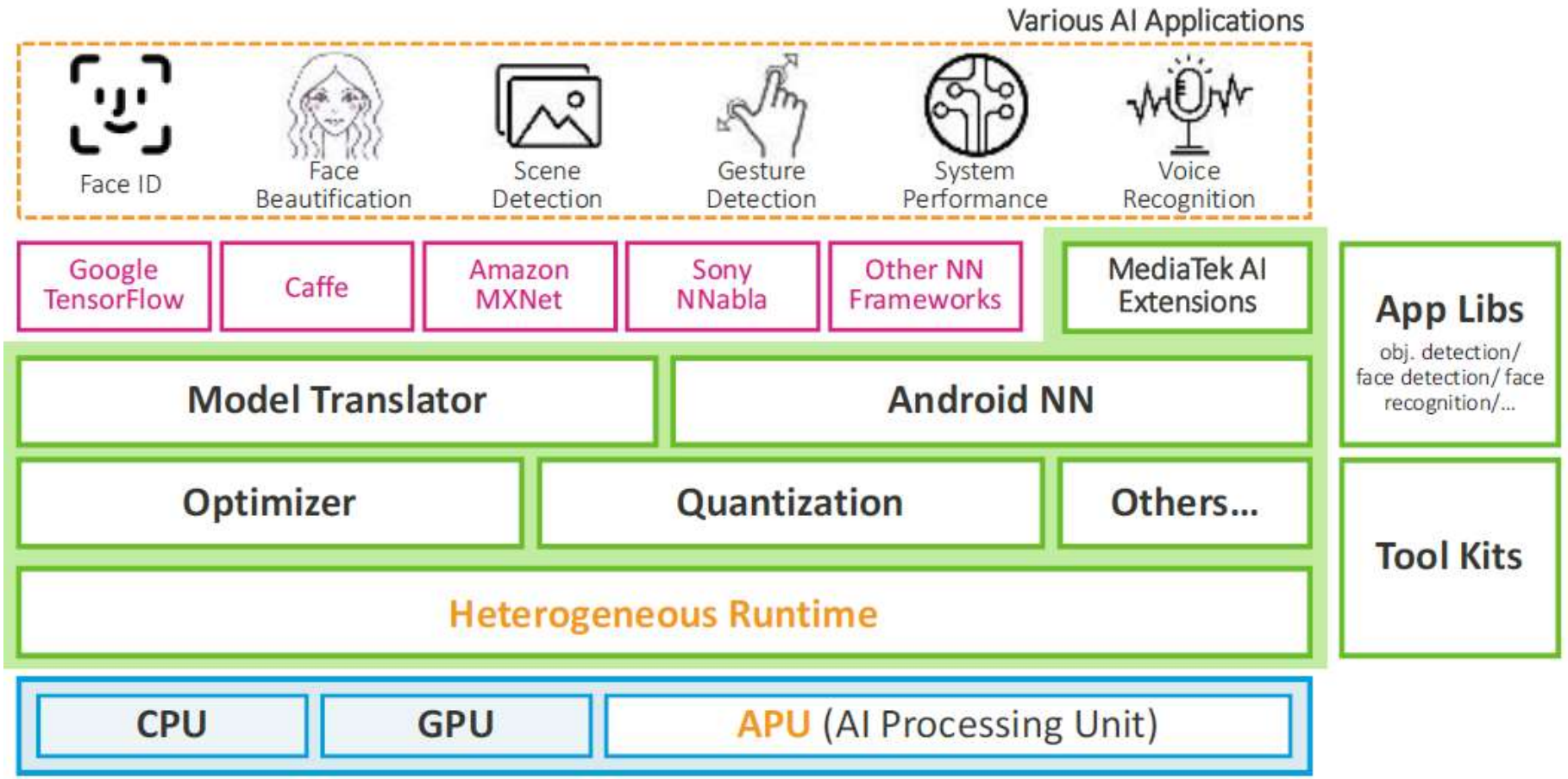
System architecture of the Android Neural Network API (Source Google) [32]



https://www.eetindia.co.in/news/article/18022704-mwc-mediatek-aims-for-upper-midrange-with-ai

2.3.3 MediaTek's Helio P midrange line (10)

MediaTek's AI support for the Helio P60 [33]



2.3.3 MediaTek's Helio P midrange line (11)

The heterogeneous runtime component in NeuroPilot software development kit (SDK) [33]

- NeuroPilot supports current state-of-the-art AI frameworks, like Google's TensorFlow, the open-source Caffe, Amazon's MXNet and Sony's NNabla.
- NeuroPilot also includes a model translator to allow programmers to enable AI applications on devices.
- In addition, application libraries are offered to allow both fast PC-based prototyping and close-to-metal performance in the Edge AI development.
- Finally, the heterogeneous runtime provides task scheduling for the CPU, GPU, and APU.

2.3.3 MediaTek's Helio P midrange line (12)

The APU (AI Processing Unit) of the Helio P60 processor [60]

It is a dual core dedicated neural network accelerator based on the licensed IP of the Tensilica Vision P6 DSP from Cadence Tensilica.

2.3.3 MediaTek's Helio P midrange line (13)

Remarks on the Cadence Tensilica DSP family

- The original design comes from Tensilica, a semiconductor IP company, like ARM.
- It was founded in 1997 by Chris Rowen, one of the founders of MIPS Technologies.
- Tensilica offered DSPs for embedded SoC designs.
- In 2013 Tensilica was acquired by Cadence Design Systems.
- An important product line of Cadence Tensilica is the Tensilica Vision DSP family.
- It has, at writing of these slides, the following three models:

Figure: Models of the Tensilica Vision DSP family [34]

2.3.3 MediaTek's Helio P midrange line (14)

The ISA, underlying the Tensilica Vision DSP family, called Xtensa [35]

- Xtensa is costumer extensible and focuses on wide (512 bits) SIMD processing.
- Xtesa allows to intermix short basic instructions with multi-operation (VLIW) instructions.

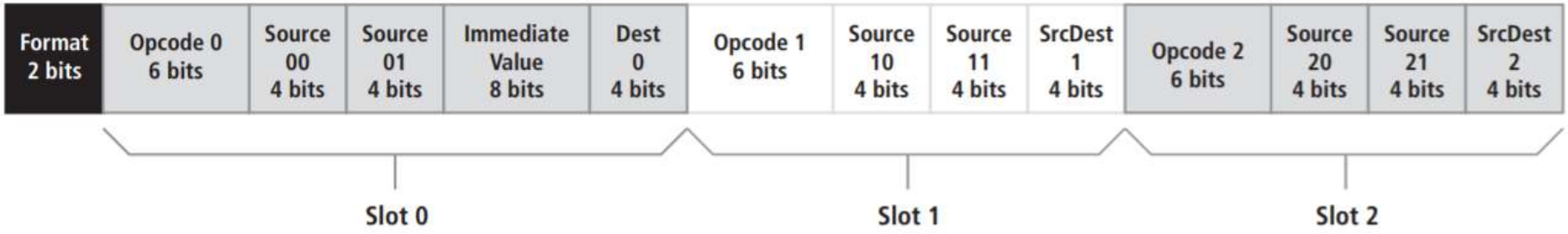


Figure: Example of a three slot VLIW instruction, each slot specifying an operation and its operands [35]

- The number of available slots is ISA version dependent, e.g. the ISA version underlying the Vision P6 has 5 VLIW slots.
- In implementations each slot can have either dedicated execution resources, like EUs, register files and data memories, or shared resources, like common register files and data memories.
- Xtensa is local memory based, there are multiple memory banks and 512-bit loads/stores.

2.3.3 MediaTek's Helio P midrange line (15)

Key features of the recent models of Tensilica Vision DSP family

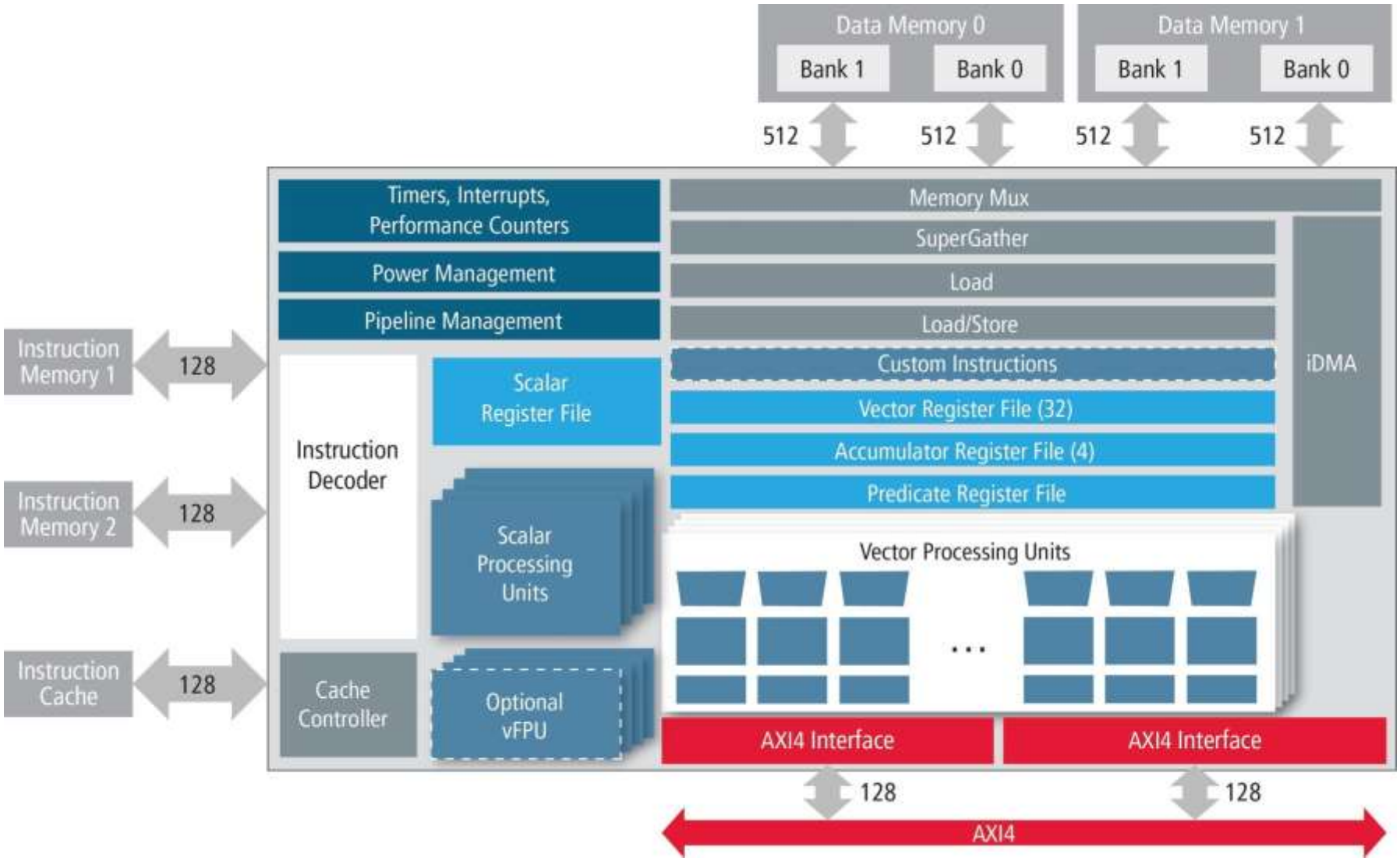
The Vision P5 DSP (2015, 16 nm)

- It aims at speeding up image processing.
- Accordingly, it supports FP32 processing, implemented in form of SIMD processing.
- With 512-bit SIMD length, up to 16 FP32 operands may be kept in a data word.
- Then assuming 4-way VLIW operation, up to 64 FP32 MAC operations ("multiplication and accumulation" operations), can be executed in parallel.
- The clock rate is 1.1 GHz.
- This results in a peak performance for FP32 operations of

$$1.1 \times 64 = 70.4 \text{ GMAC/s}.$$

- The Helio X30 processor includes the Vision P5 DSP for speeding up image processing.

Block diagram of the Vision P5 DSP [36]



2.3.3 MediaTek's Helio P midrange line (17)

The Vision P6 DSP (2016, 16 nm)

- It aims at speeding up image and AI processing.
- It has introduced FP16 data types and operations.
- With 512-bit long SIMD data, each data word includes up to 32 FP16 operands.
- Then for a 4-way VLIW operation up to 128 FP16 MAC operations, (multiply and accumulate operations) can be executed in parallel.
- The clock rate is 1.1 GHz.
- This result in a peak performance for FP16 operations of

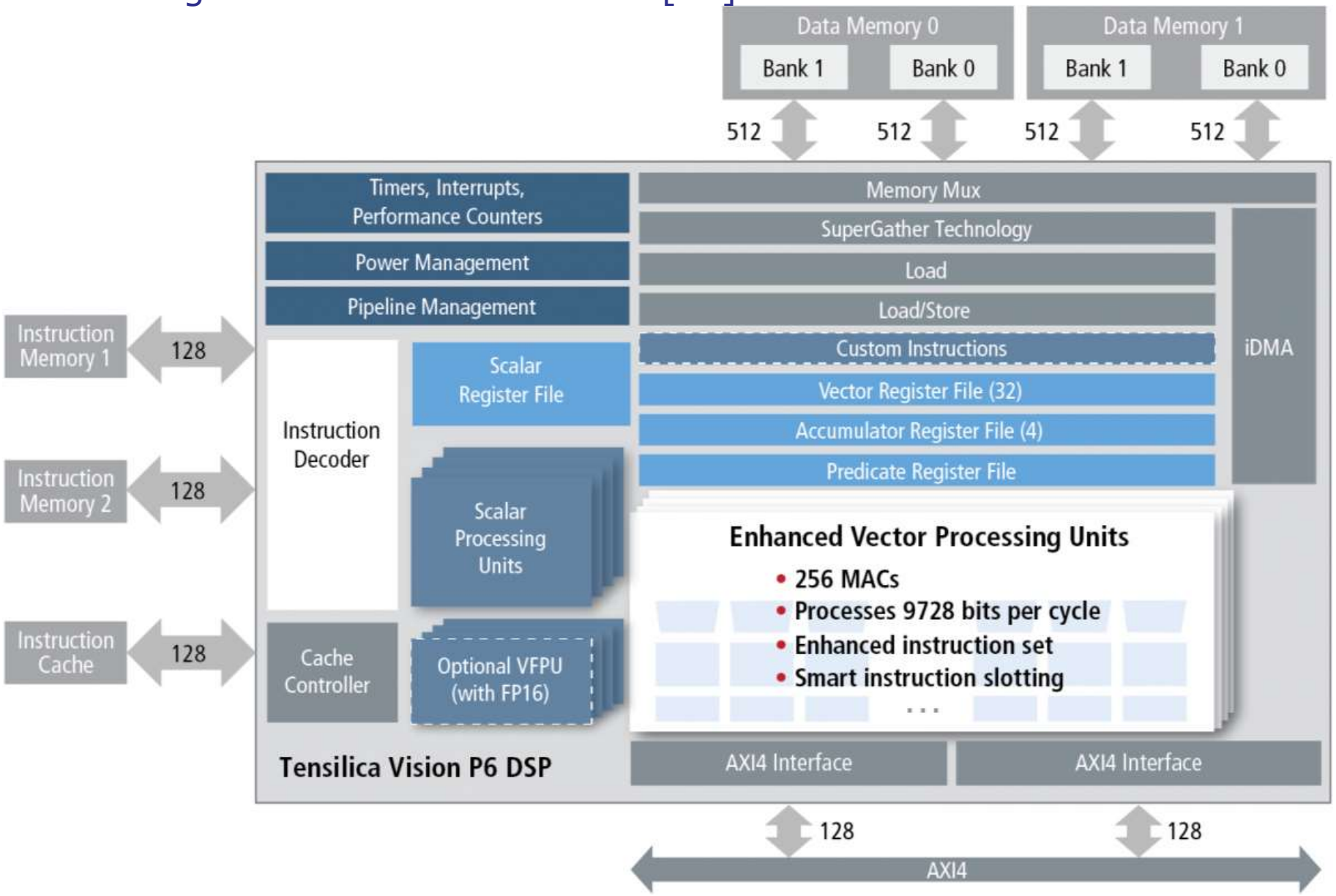
$$1.1 \times 128 = 140.8 \text{ GMAC/s}.$$

- The Helio P60 processor includes two Vision P6 DSP cores, providing

$$2x\ 140.8 = 280.8 \text{ GMAC/s performance.}$$

- As far as FX8 operations are concerned, a SIMD word can keep 64 operands, then for four VLIW slots 4x64 = 256 MAC operations can be performed in a cycle.

Block diagram of the Vision P6 DSP [37]



The Vision Q6 DSP (2018, 16 nm) -1

- It aims at speeding up image and AI processing.
- It is the 5. gen. DSP and has an enhanced architecture with 1.5 GHz clock rate.
- With the increasing role of AI processing FX8 processing is gaining in importance, since accuracy requirements allow using short, even FX8 data types, as the Figure below indicates it.

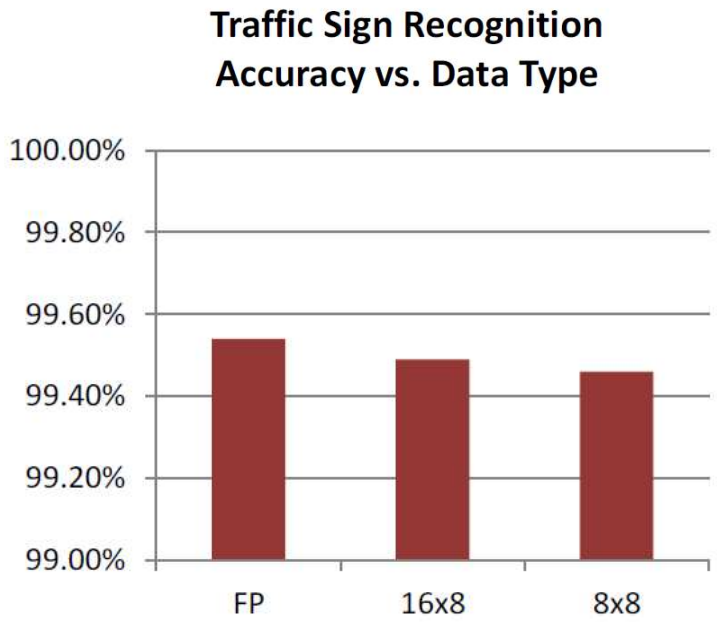


Figure: Impact of the data type to accuracy in calculating inferences [38]

The Vision Q6 DSP (2018, 16 nm) -2

- In case of FX8 data, 512-bit long SIMD words include up to 64 FX8 operands.
- Then assuming 4 VLIW slots with dedicated resources, up to 256 FX MAC operations, (multiply and accumulate operations) can be executed in parallel.
- With the clock rate of 1.5 GHz, this results in a peak performance for FX8 operations of

$$256 \times 1.5 = 384 \text{ GMAC/s.}$$

- It can be assumed that the Helio P90 processor includes three Vision Q6 DSP cores, providing

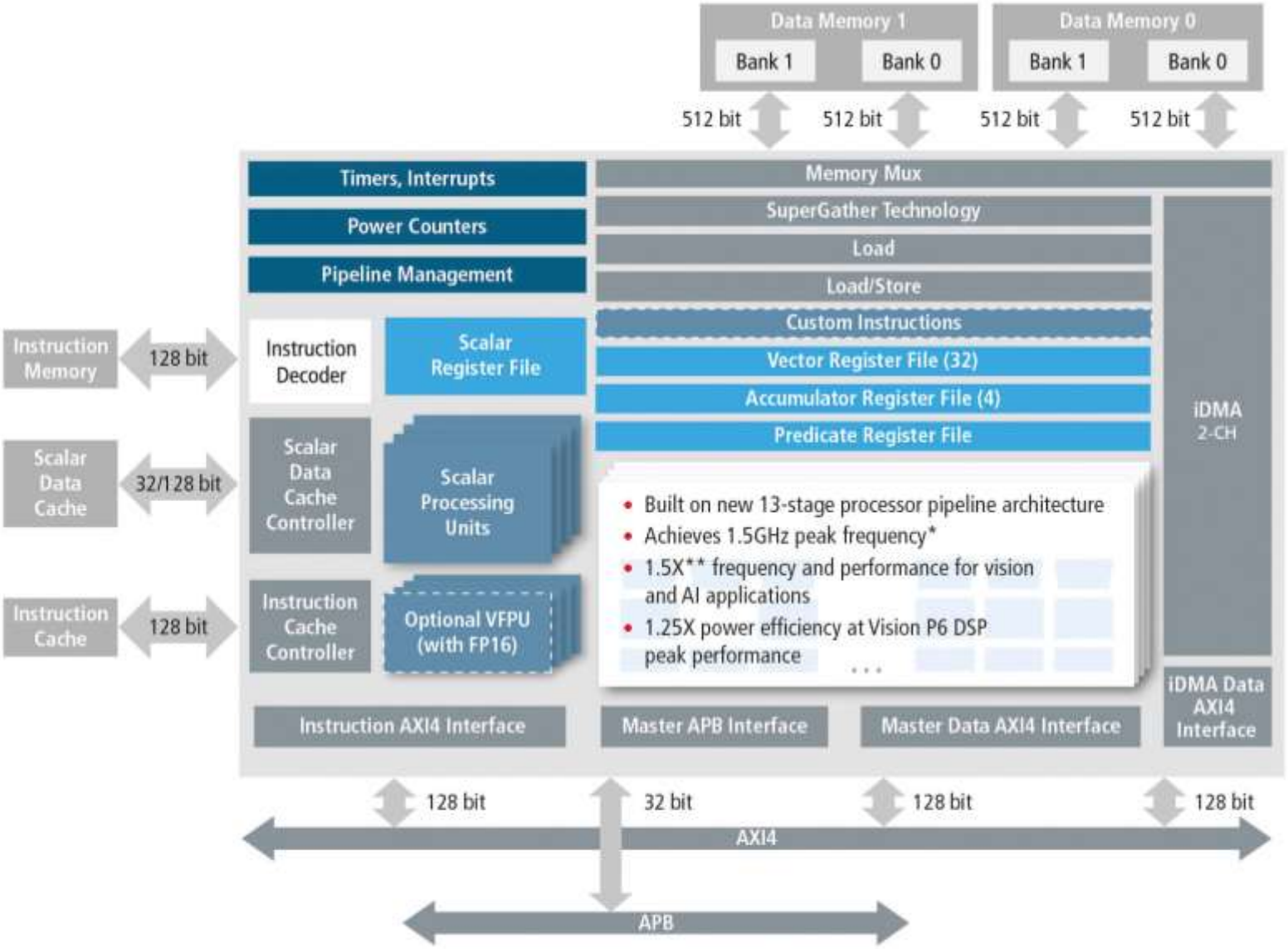
$$3x\ 384 = 1152 \text{ GMAC/s performance.}$$

Nevertheless, the official performance figure is 1127 GMAC/s.

Note that the peak performance values for the P5, P6 and Q6 DSPs are specified differently:

- in case of the P5 for FP32 operations,
- in case of the P5 for FP16 operations, and
- in case of the Q6 for FX8 operations.

Block diagram of the Vision Q6 DSP [39]



2.3.3 MediaTek's Helio P midrange line (22)

Note that the Vision Q6 has three master AXI4 interfaces instead of two (in the P5 and P6 DSP) to alleviate memory bandwidth challenges in vision and AI applications [39].

Interconnecting multiple Q6 units, called cores

Multiple Vision Q6 cores are attached to the interconnect via AXI4 buses, as shown below.

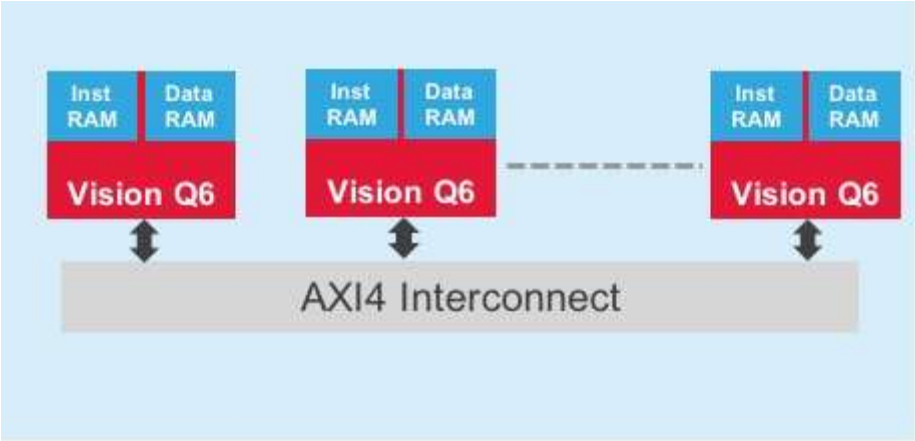
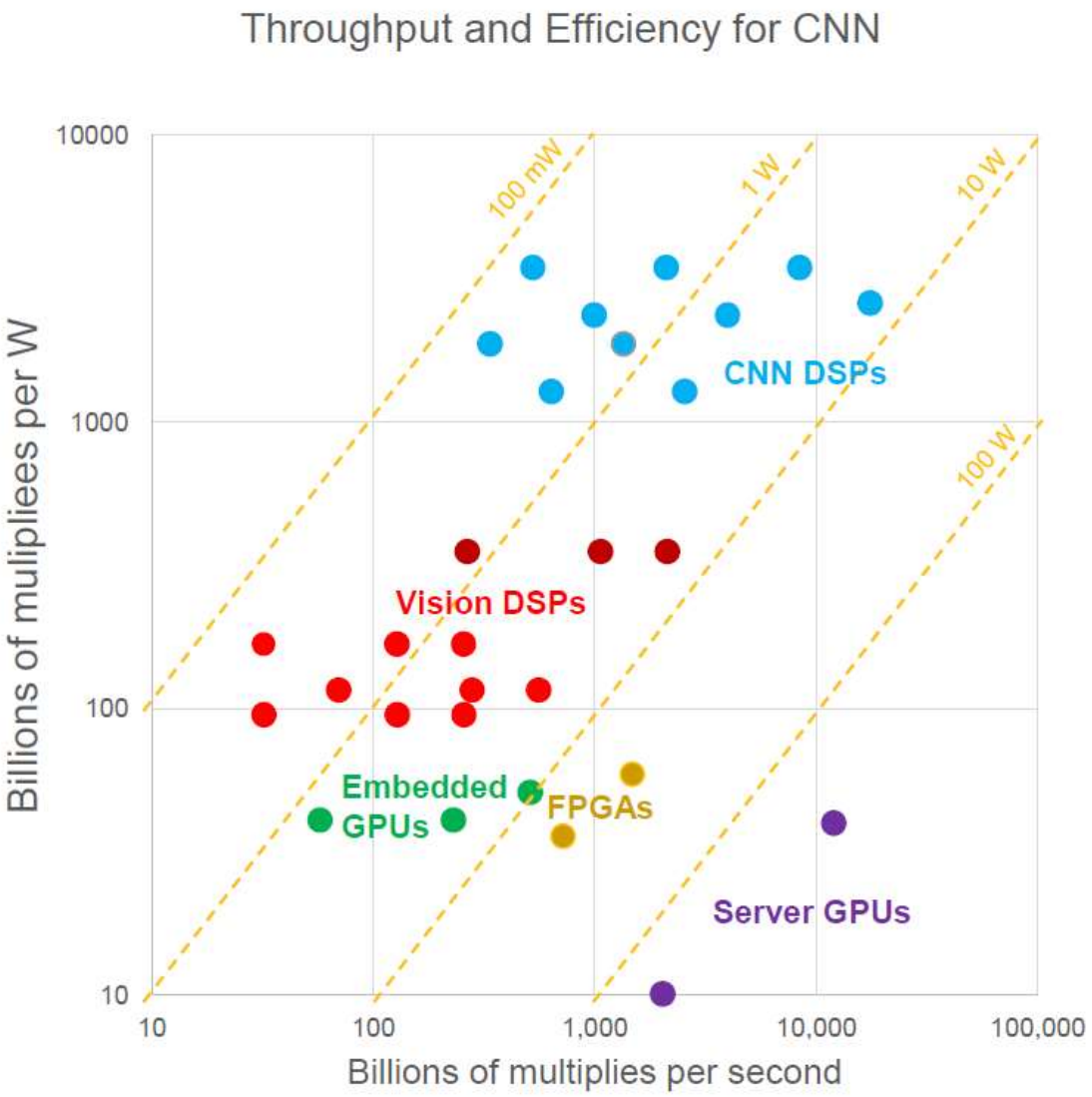


Figure: Using multiple Vision Q6 cores in a SoC [40]

2.3.3 MediaTek's Helio P midrange line (24)

Motivation for using CNN DSPs for AI [38]



2.3.3 MediaTek's Helio P midrange line (25)

Example 2: The Helio P90 midrange model

- It is MediaTek's first processor built on the Cortex A-75/A55 cores that support ARMc8.2 and ARM's DynamIQ core cluster concept.
- Announced in 12/2018, to be launched in Q1/2019.
- It includes an upgraded APU (APU 2.0) with a peak performance of 1127 MAC/s for FX8 operations.

Main features of MediaTek's Helio P90 [41]

SoC	Helio P90	Helio P60/P70
CPU	2x Cortex A75 @ 2.2GHz 6x Cortex A55 @ 2.0GHz	4x Cortex A73 @ 2.0/2.1GHz 4x Cortex A53 @ 2.0GHz
GPU	PowerVR GM 9446 @ 970MHz	Mali G72MP3 @ 800/900MHz
APU / NPU / AI Proc. / Neural IP	2x +140GMACs (Tensilica DSP) + In-house Inference Engine 1127GMACs total	2x 140GMACs (Tensilica DSP)
Memory	2x 16bit LPDDR4X @ 1866MHz	1x 32bit LPDDR3 @ 933MHz 2x 16bit LPDDR4X @ 1800MHz
ISP/Camera	1x 48MP or 2x 24+16MP	1x 32MP or 2x 20+16MP
Encode/ Decode	2160p? H.264 & HEVC	2160p30 H.264 & HEVC
Integrated Modem	Category 12/13 DL = 600Mbps 3x20MHz CA, 256-QAM, 4x4 MIMO UL = 150Mbps 2x20MHz CA,64-QAM	Category 7/13 DL = 300Mbps 3x20MHz CA, 64-QAM UL = 150Mbps 2x20MHz CA,64-QAM
Mfc. Process	12FFC	12FFC

2.3.3 MediaTek's Helio P midrange line (27)

Benefits of the APU 2.0 dedicated AI unit [42]

APU 2.0

- AI performance leadership: 1127 GMACs
  - 4X more powerful than previous generation P series
  - 50% faster than high-end competitor SoC
- 10-20% faster at INT8
- Greater power efficiency at FP16

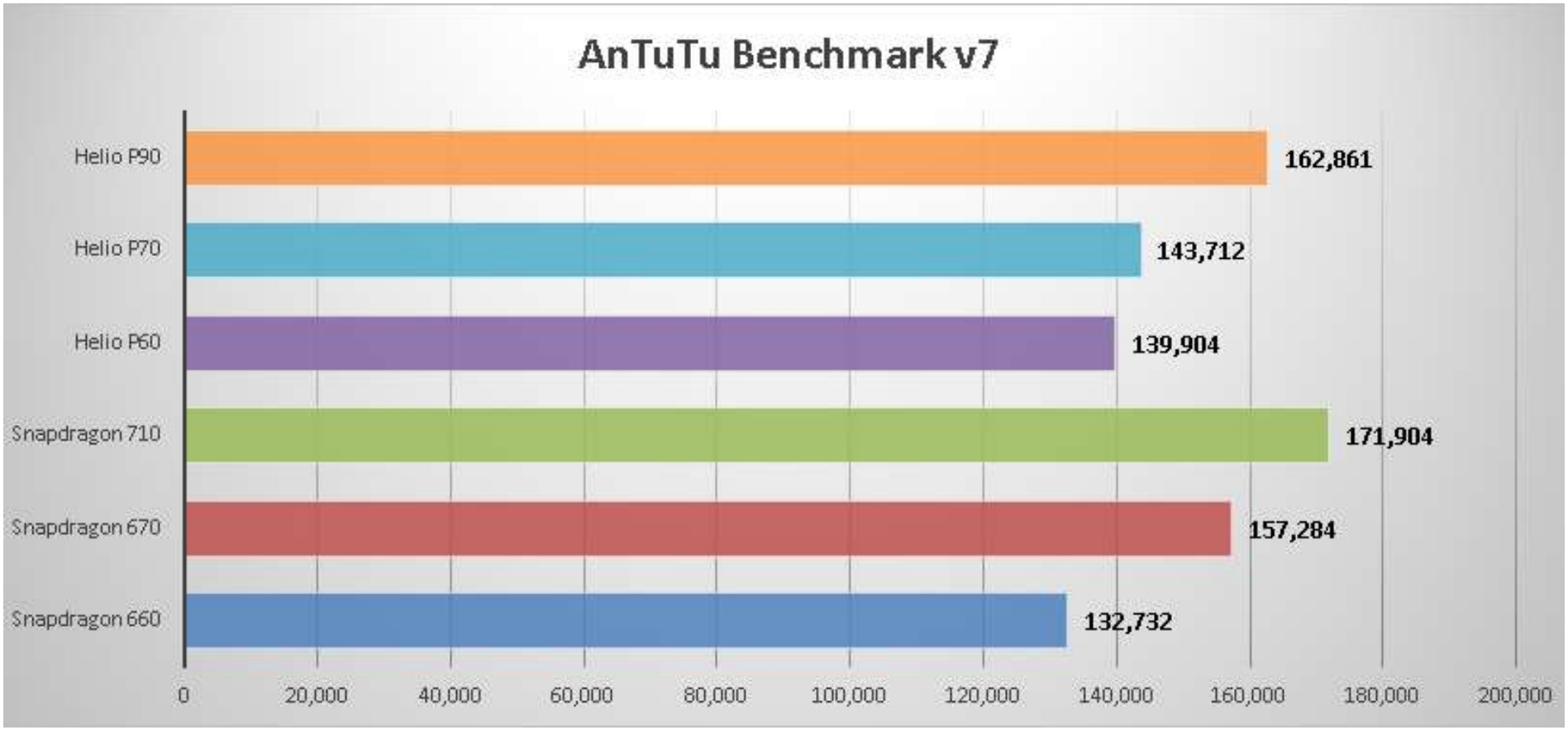
AI-accelerated experiences

- 5-person human pose tracking
- Full body avatar AR
- 3D pose tracking
- Multiple object identification (Google Lens)
- AR/MR acceleration
- Semantic segmentation
- Scene identification

	MediaTek Helio P90
AI	MediaTek APU 2.0
CPU	Octa-Core: 2x ARM Cortex-A75 @ 2.2GHz; 6x ARM Cortex-A55 @ 2.0GHz
GPU	IMG PowerVR GM 9446 GPU up to 970MHz
Memory	2-Channel LPDDR4x up to 8GB, 1866MHz
Storage	UFS 2.1
Camera	48MP or 24+16MP
Display	2520 x 1080 (Full HD+) at 21:9
Modem	4G LTE Cat-12 (DL) / Cat-13 (UL) (FDD/TDD), 4x4 MIMO, 3CA, 256QAM, HPUE, IMS (VoLTE\ ViLTE\WFC), eMBMS, Dual 4G VoLTE (DSDS), Band 71, TAS 2.0
Connectivity	802.11 a/b/g/n/ac, Bluetooth 5.0, GPS + Glonass + Beidou + Galileo, FM radio

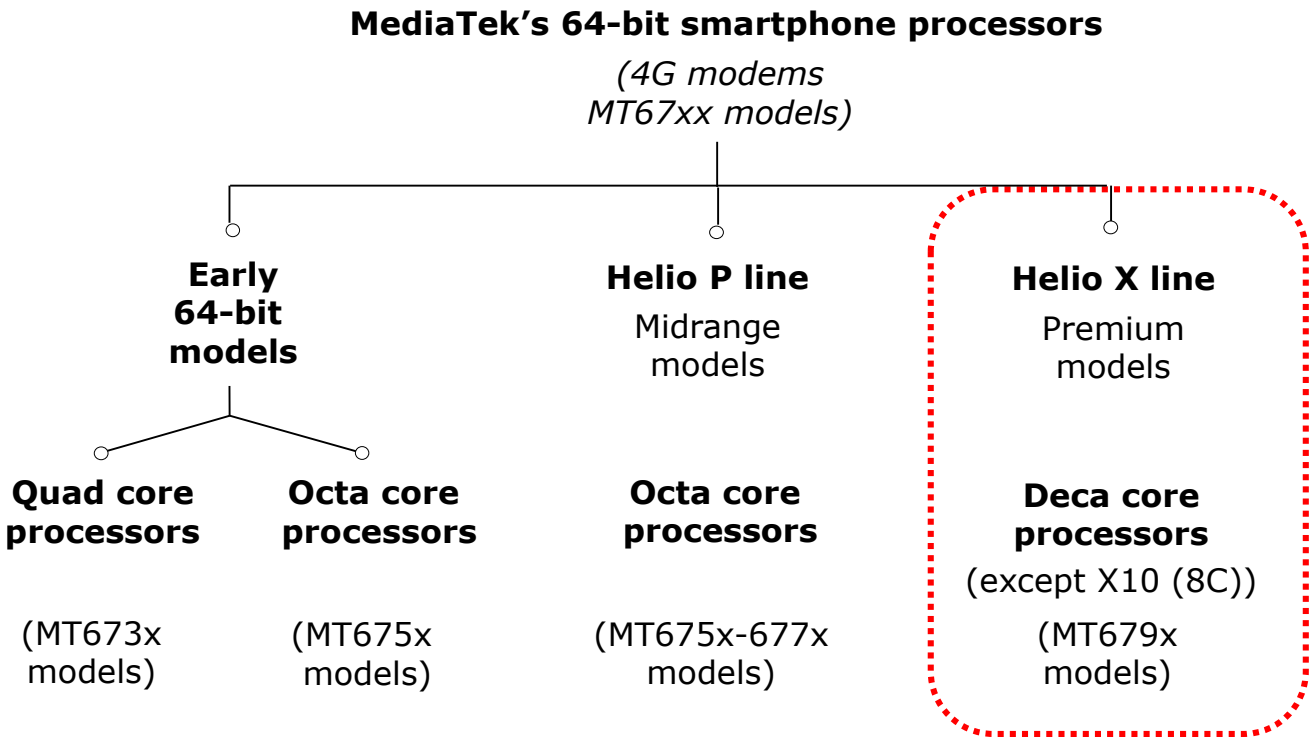
2.3.3 MediaTek's Helio P midrange line (28)

Contrasting the performance of the P90 with comparable mid-range processors, based on the AnTuTu Benchmark v7 scores [43]



2.3.4 MediaTek’s Helio X high-end line

2.3.4 MediaTek’s Helio X high-end line



2.3.4 MediaTek’s Helio X high-end line (2)

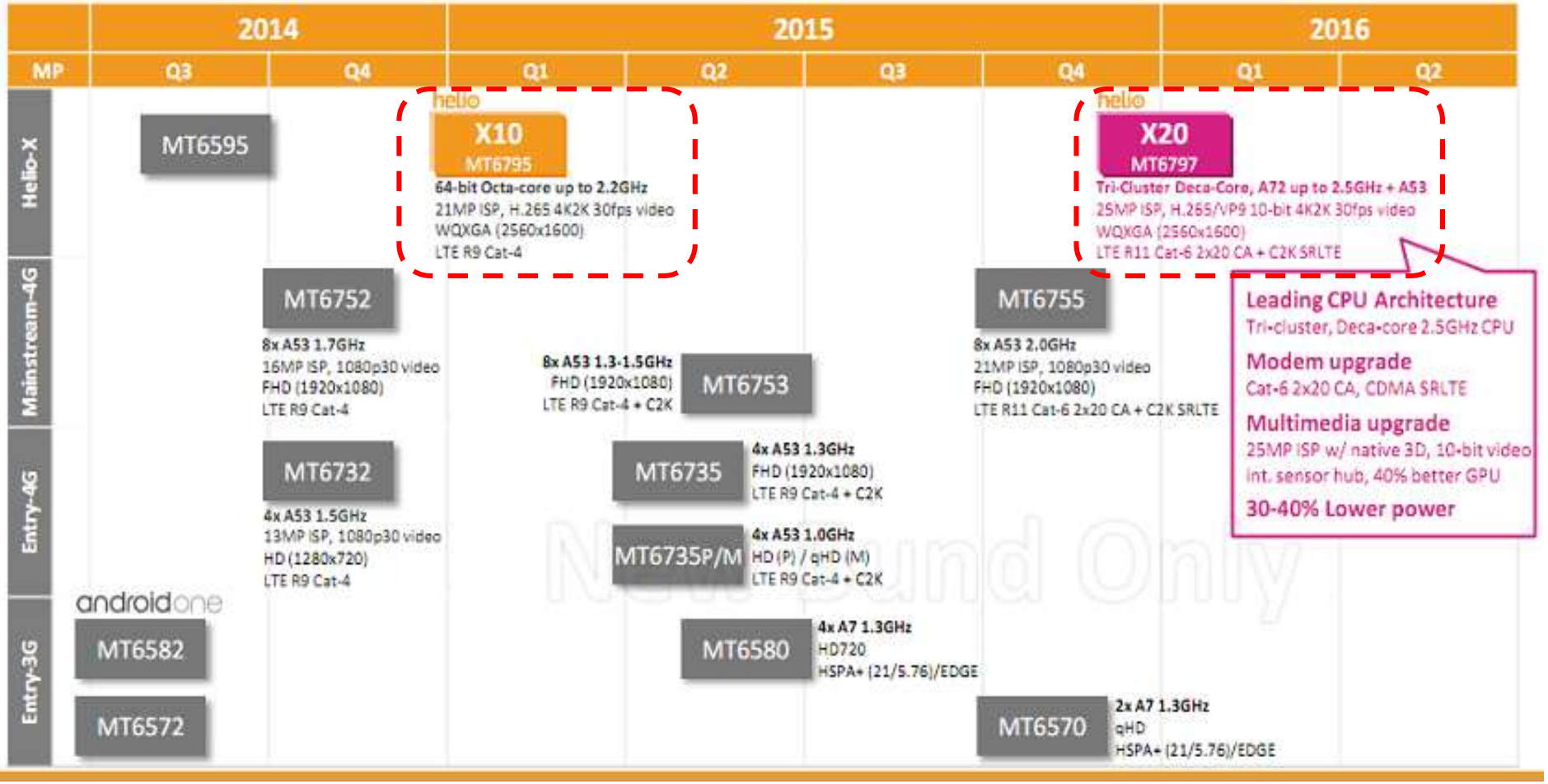
Overview of MediaTek's Helio X-line -1

The first two models of the Helio X-line, the X10 and X20 were presented on MediaTek's smartphone product roadmap for 2014 - 2016 [3].

They were identified as 64-bit octa core and deca core high-end models, as seen in the next Figure.

2.3.4 MediaTek's Helio X high-end line (3)

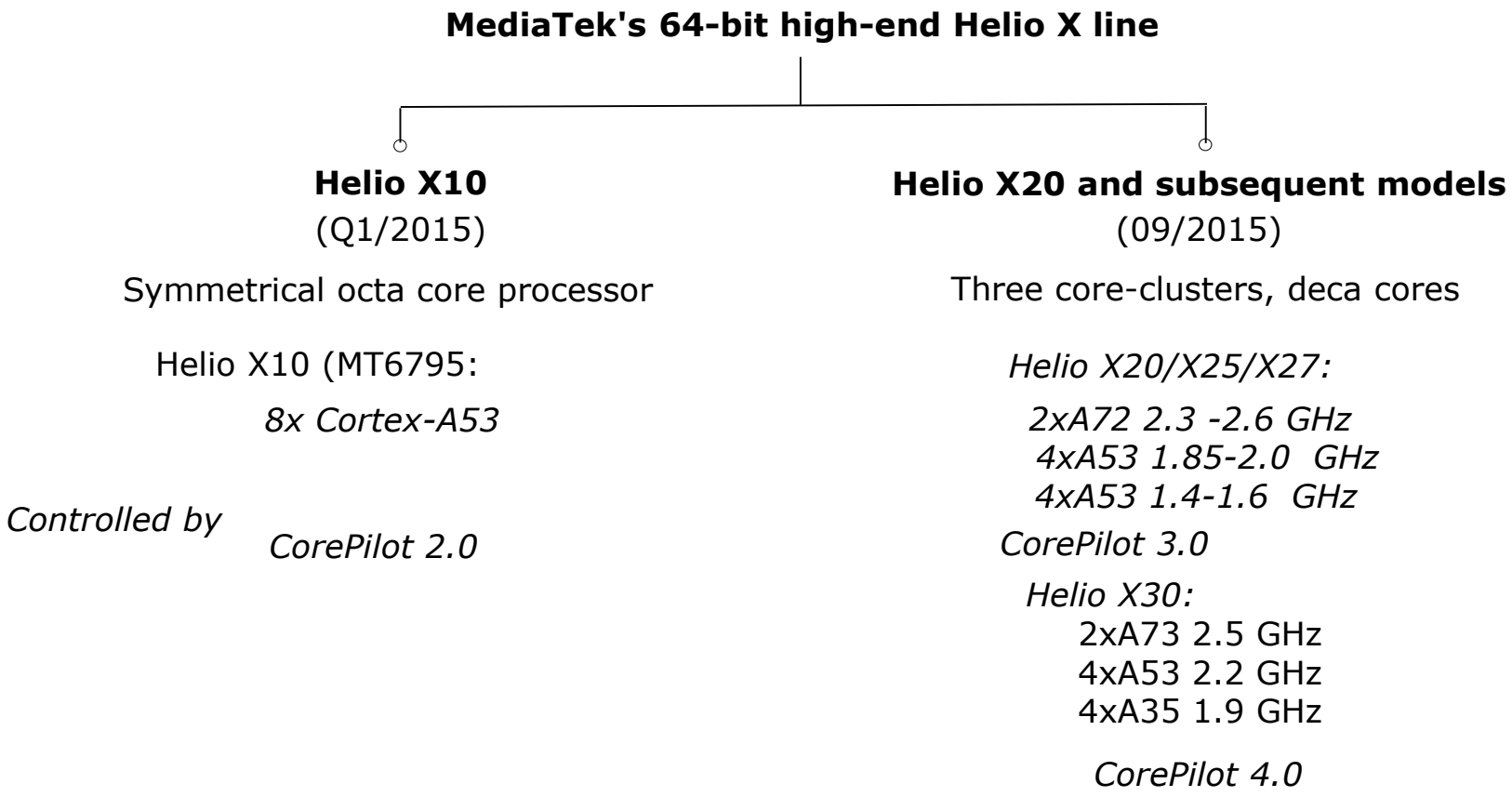
The Helio X line on MediaTek's 2014-2016 smartphone product roadmap [3]



2.3.4 MediaTek’s Helio X high-end line (4)

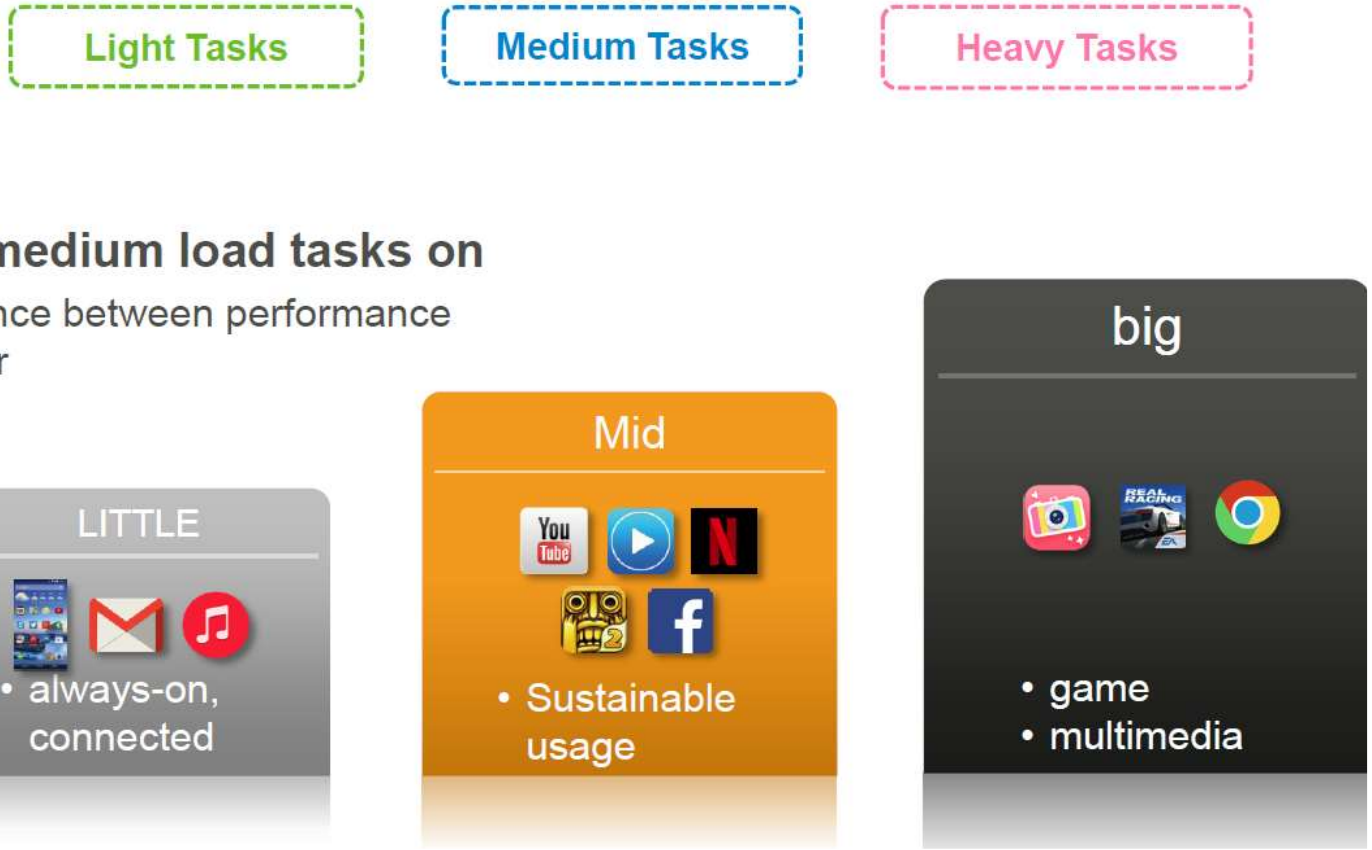
Overview of MediaTek's Helio X-line -2

As long as the Helio X10 model was an octa core SMP model, beginning with the X20, the Helio X-line became a three core cluster, deca core design, as indicated below.



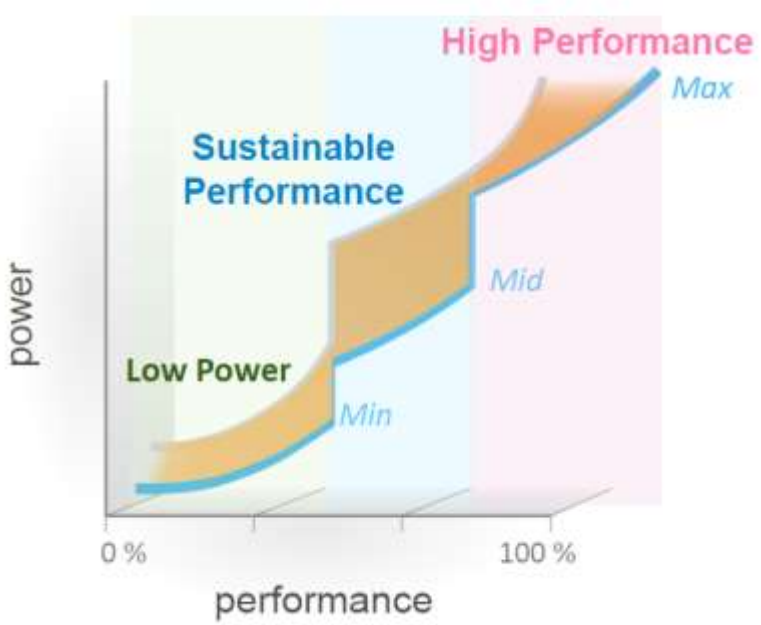
2.3.4 MediaTek's Helio X high-end line (5)

Light, medium and big workloads [29]



2.3.4 MediaTek's Helio X high-end line (6)

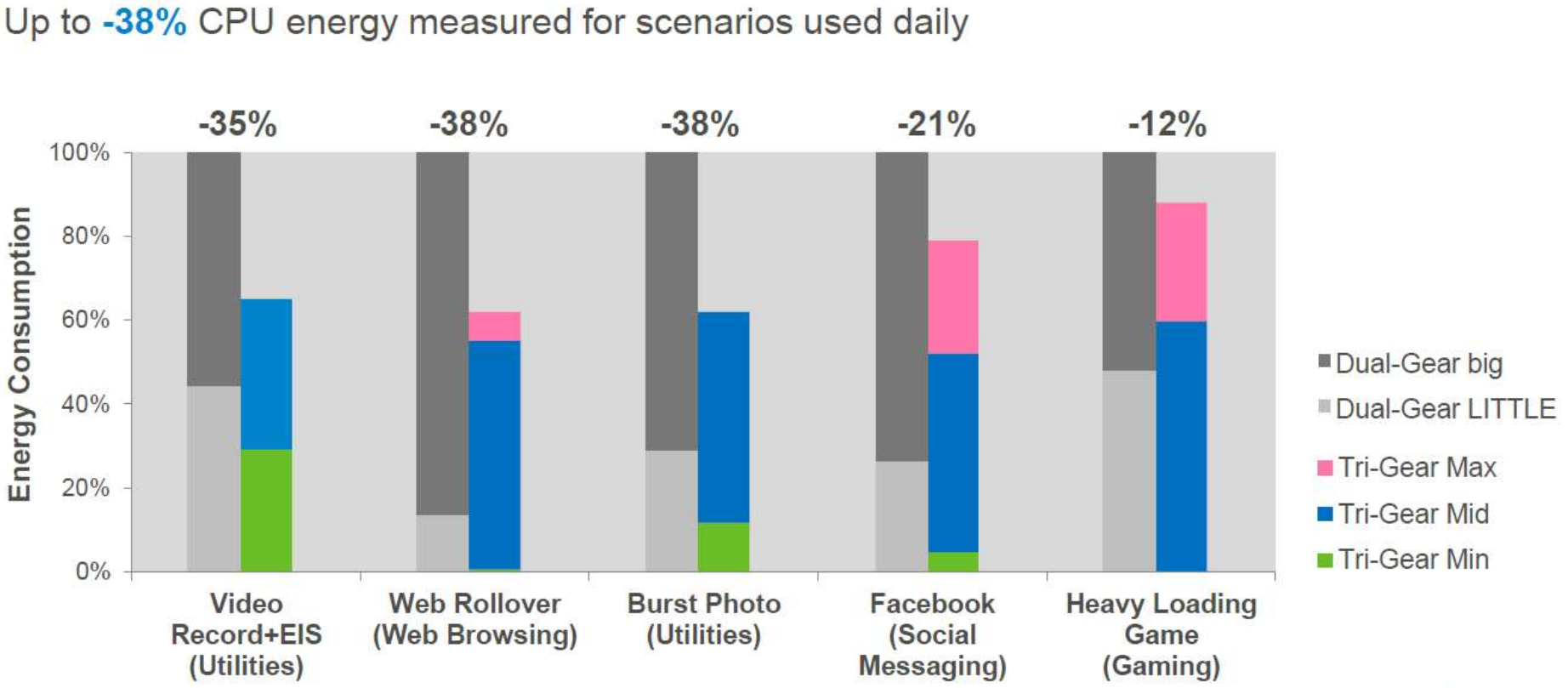
Introduction to 3-core cluster processors [29]



1. New **Mid** gear introduced
2. **Min** gear goes for even lower power, **Max** gear aims for higher performance
3. Reduced power consumption across entire performance range

2.3.4 MediaTek's Helio X high-end line (7)

Energy saving with 3-cluster (called also three-gear) design over the 2-cluster (dual-gear) design [29]



2.3.4 MediaTek's Helio X high-end line (8)

Key features of the high-performance Helio X line [3]

Model	Launched	Techn.	Configura-tion	GPU	Memory (POP)	Connect. up to	CorePilot version
Helio X10 (MT6795)	Q1/2015	28 nm	8xA53 2.0 GHz	IMG G6200 700 MHz	2xLPDDR3 933 MHz	LTE cat. 4	CorePilot (2.0)
Helio X20 (MT6797)	05/2015	20 nm	2xA72 2.3 GHz 4xA53 1.85 GHz 4xA53 1.4 GHz	Mali T880? 780 MHz	2xLPDDR3 933 MHz	LTE cat. 6	CorePilot 3.0
Helio X25 (MT6797T)	Q2/2016	20 nm	2xA72 2.5 GHz 4xA53 2.0 GHz 4xA53 1.4 GHz	Mali 850 MHz	2xLPDDR3 933 MHz	LTE cat. 6	CorePilot 3.0
Helio X27 (MT6797X)	12/2016	20 nm	2xA72 2.6 GHz 4xA53 2.0 GHz 4xA53 1.6 GHz	Mali T880 MT4 875 MHz	2xLPDDR3 800 MHz	LTE cat. 6	CorePilot 3.0
Helio X30 (MT6799)	8/2016 In devices: 02/2017	10 nm	2xA73 2.5 GHz 4xA53 2.2 GHz 4xA35 1.9 GHz	IMG 7XTP-MT4 800 MHz	4xLPDDR4x 1866 MHz 16-bit	LTE cat. 10	CorePilot 4.0
Helio X35	Planned, but not launched						

2.3.4 MediaTek's Helio X high-end line (9)

Example 1: The Helio X20 (MT6797) model (2015)

- It has three core clusters.
- The first core cluster includes dual A72s running at 2.5 GHz.
- Both the second and third core clusters have four cores each, operating at 2.0 GHz and 1.4 GHz, respectively, as indicated in the Figure below.
- The Helio X20 was announced in 09/2015, launched in mobiles in 11/2015.

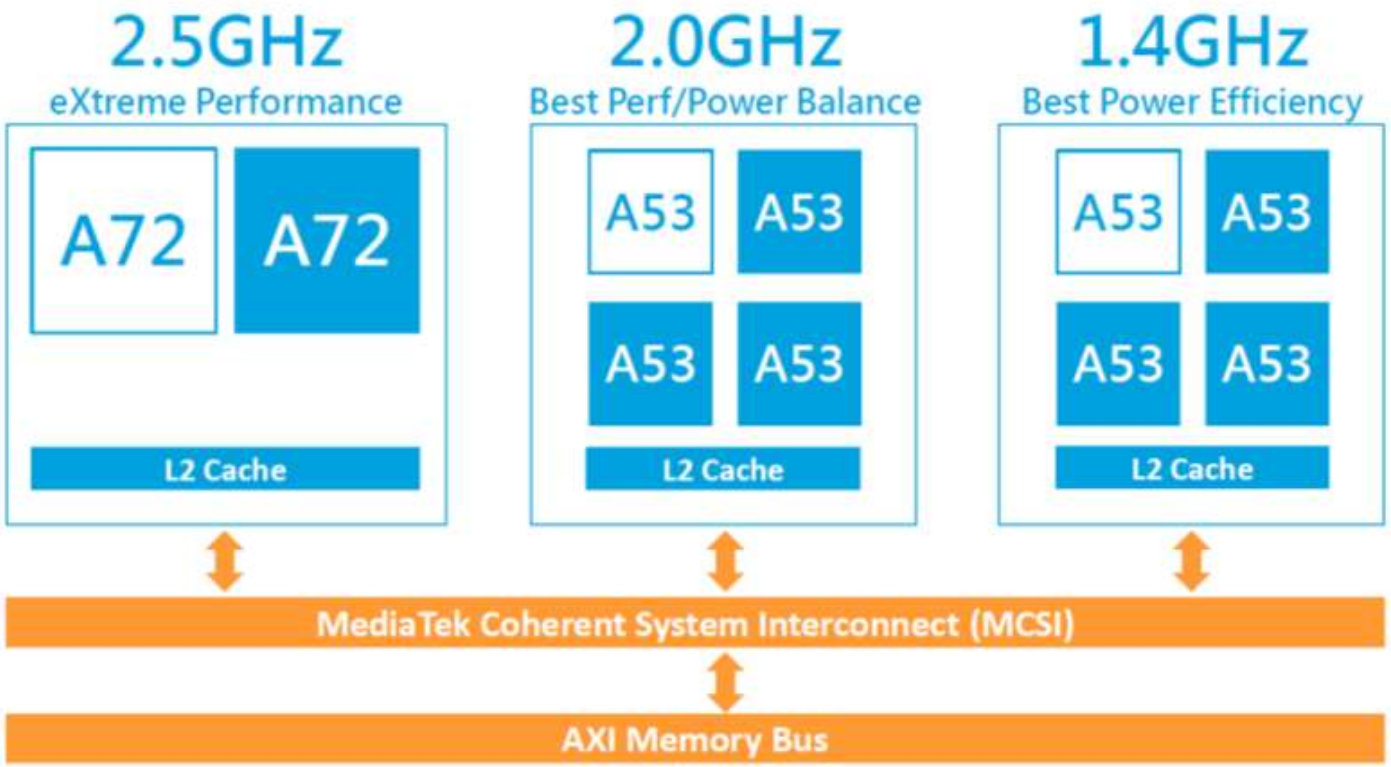


Figure: Three core clusters of the Helio X20 [23]

2.3.4 MediaTek's Helio X high-end line (10)

MediaTek's first custom interconnect, the MediaTek Coherent System Interconnect (MCSI) [21]

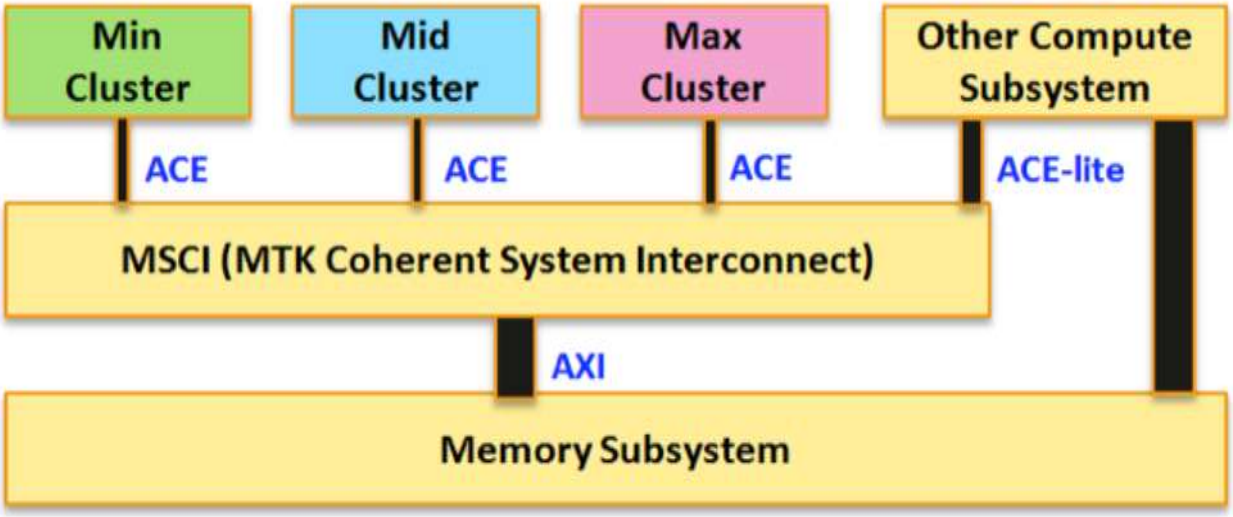


Figure 15 Tri-Cluster+MCSI Block Diagram

It was introduced along with the Helios X20, in 2015.

2.3.4 MediaTek's Helio X high-end line (11)

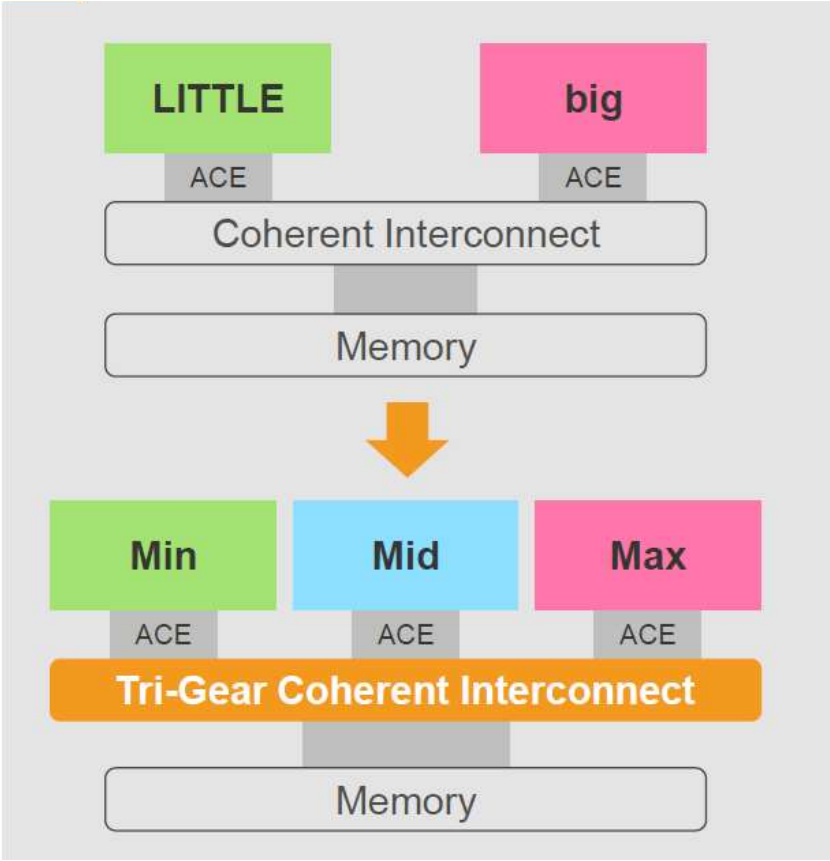
Evolution of the Coherent interconnect from the previous design [29]

Previous interconnect design:

- ARM's CCI-500 with dual ACE ports.

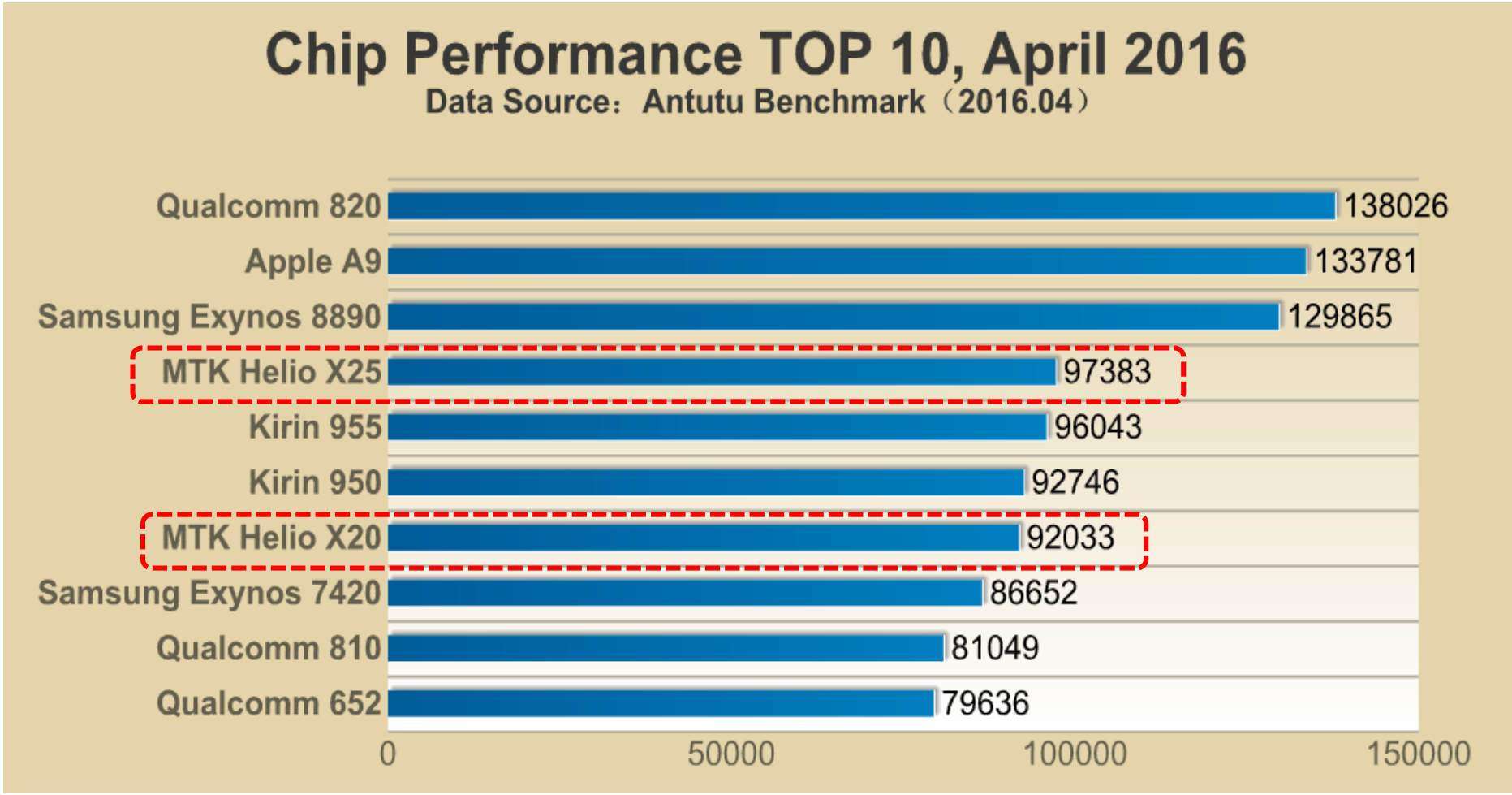
X20's interconnect design:

- Custom interconnect, called MediaTek Coherent System Interconnect MCSI) with three ACE ports
- Enhancement from 2 ACE ports to 3 ACE ports
- In addition, MediaTek introduced Fine Grain Clock Gating to reduce power consumption (~50 % reduction).



2.3.4 MediaTek's Helio X high-end line (12)

Antutu benchmark figures of the Helio X20 (MT6797) and X25 (MT6797T) models ([11]



Example 2: The Helio X30 (MT6799) model (2017)

- It is at the time being MediaTek's last Helio X series model.
- It makes use of three core clusters with dual A73, quad A53 and quad A53 cores.
- The clusters operate at 2.5, 2.2 and 1.9 GHz, respectively.

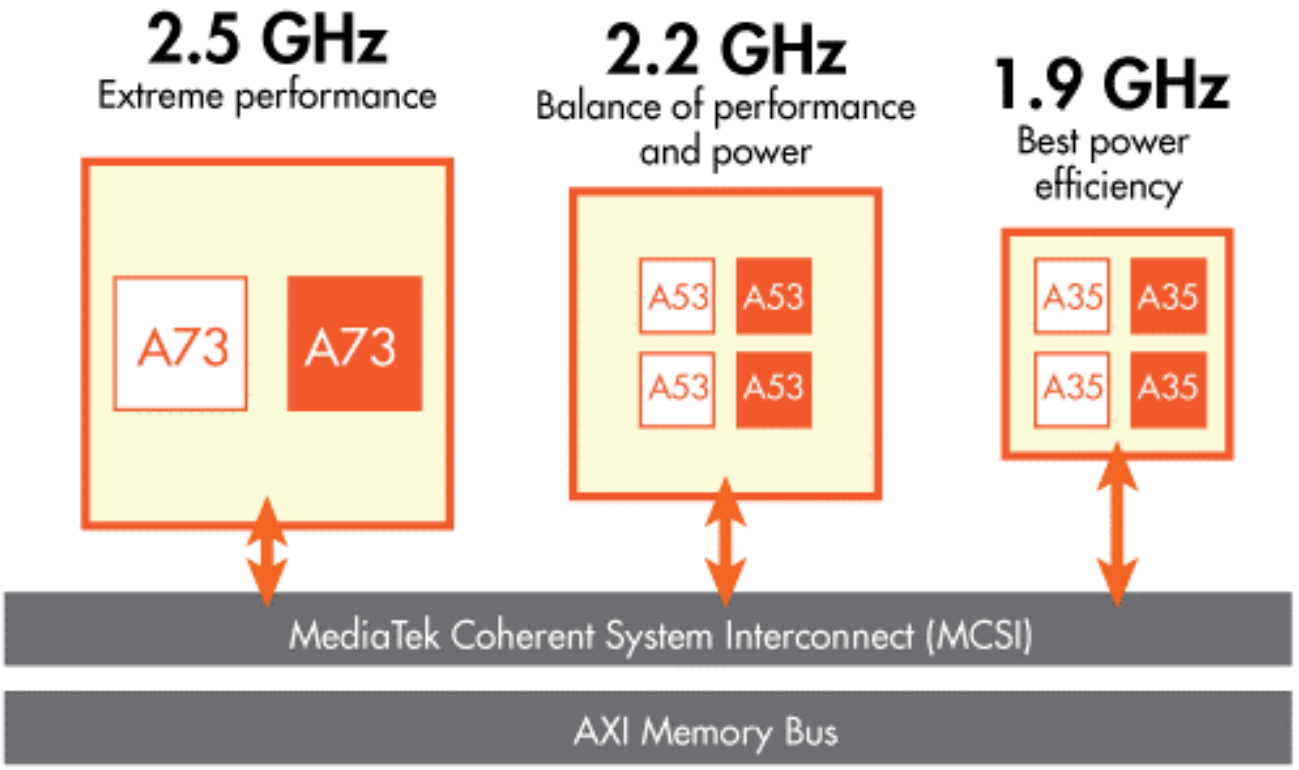


Figure: Simplified block diagram of Helio X30 [44]

2.3.4 MediaTek's Helio X high-end line (14)

Enhanced image processing in the X30

- Image processing is enhanced by introducing Cadence Tensilica's Vision P5 DSP and offloading vision processing load from the CPU and GPU.
- The vision P5 has a peak performance of 70 GMAC/s.

MAC: Multiply-Accumulate operation

2.3.4 MediaTek's Helio X high-end line (15)

Shifting Mediatek's focus from high-end (premium) smartphone processors (X-line) to midrange (P-line) processors [45]

- As long as Mediatek's midrange P-line processors were widely used worldwide in 2017, their X-line processors were only marginally, (by a few Chinese OEMs).
- As a consequence, in Q4/2017 Mediatek shifted their focus from the high-end (premium) smartphone processors (Helio X-line) to midrange (Helio P-line) processors.
- Nevertheless, Mediatek will continue developing high-end smartphones.

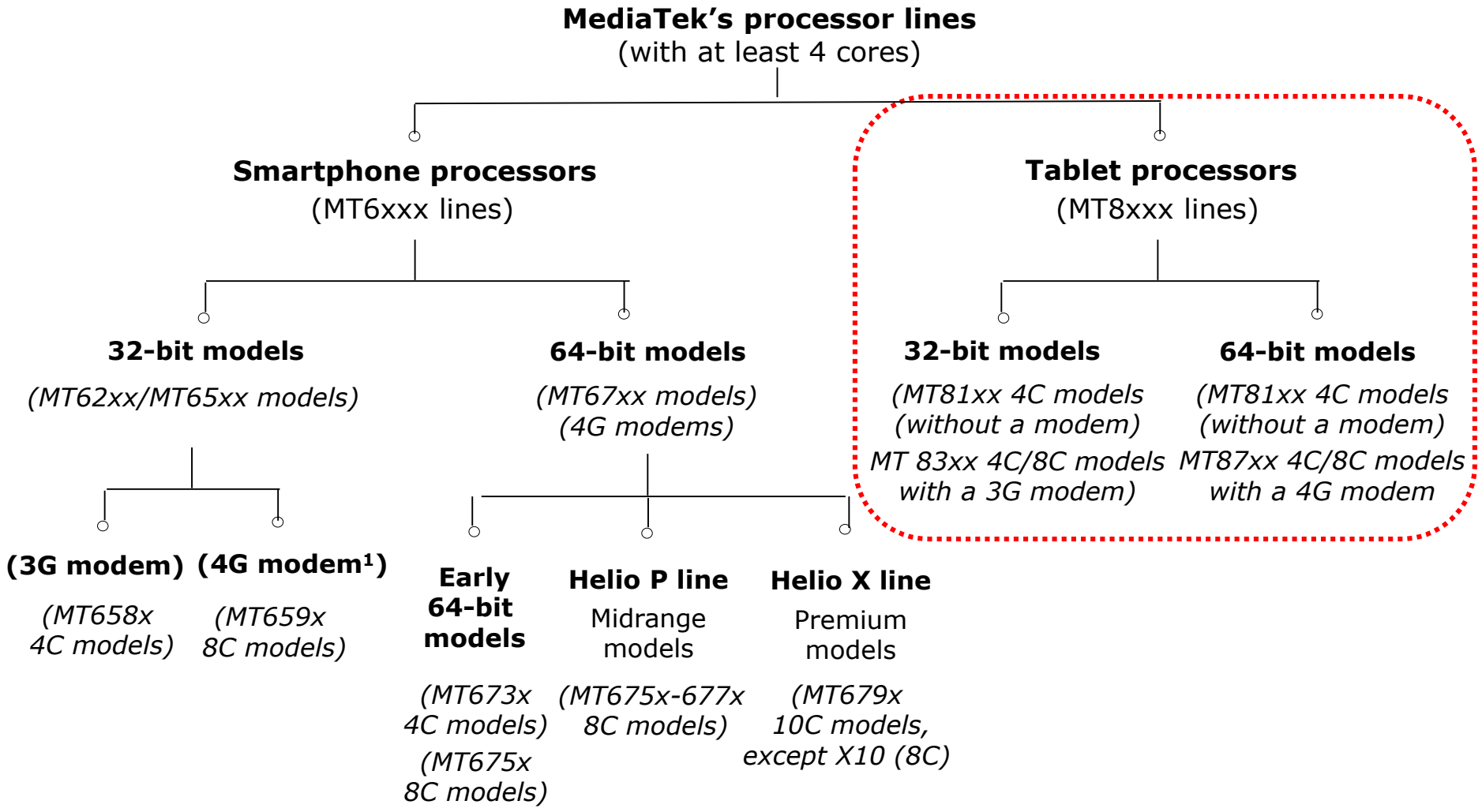
3. MediaTek’s tablet processors

- 3.1 Overview
- 3.2 MediaTek’s 32-bit tablet processors
- 3.3 MediaTek’s 64-bit tablet processors

3.1 Overview

3. MediaTek's tablet processors

3.1 Overview -1

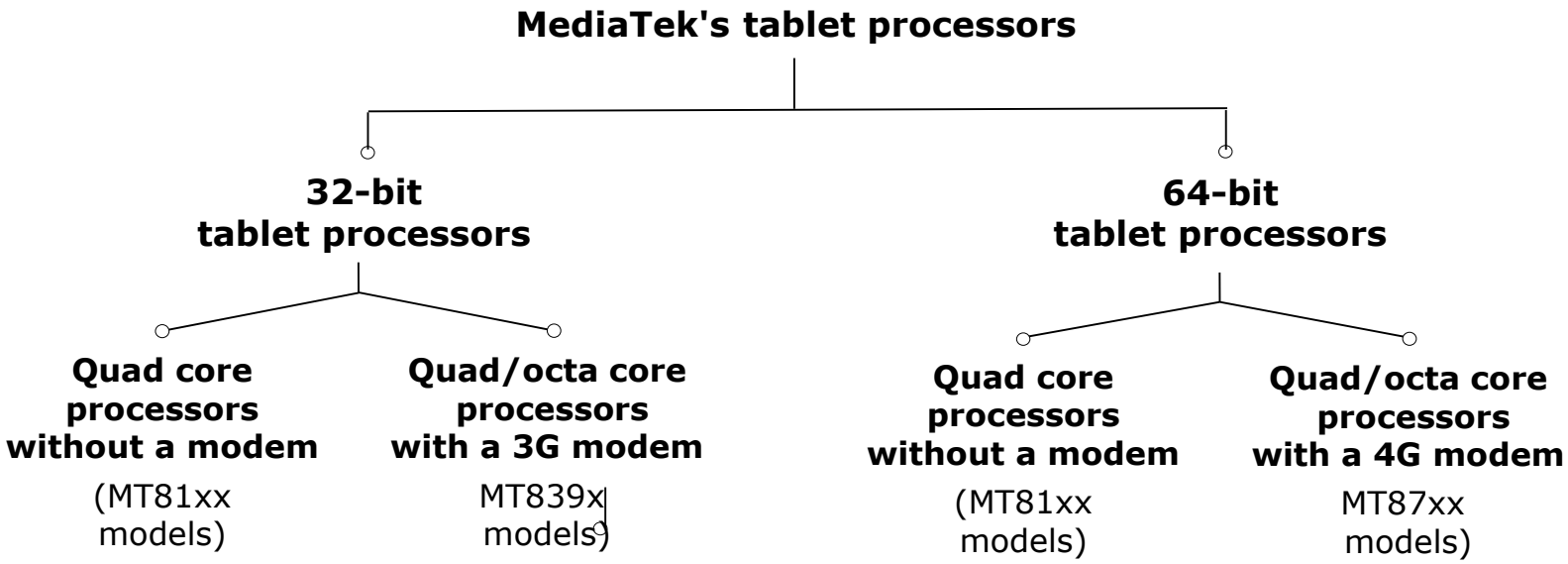


[1]The MT6591/MT6592 models need an external modem to provide LTE

Overview -2

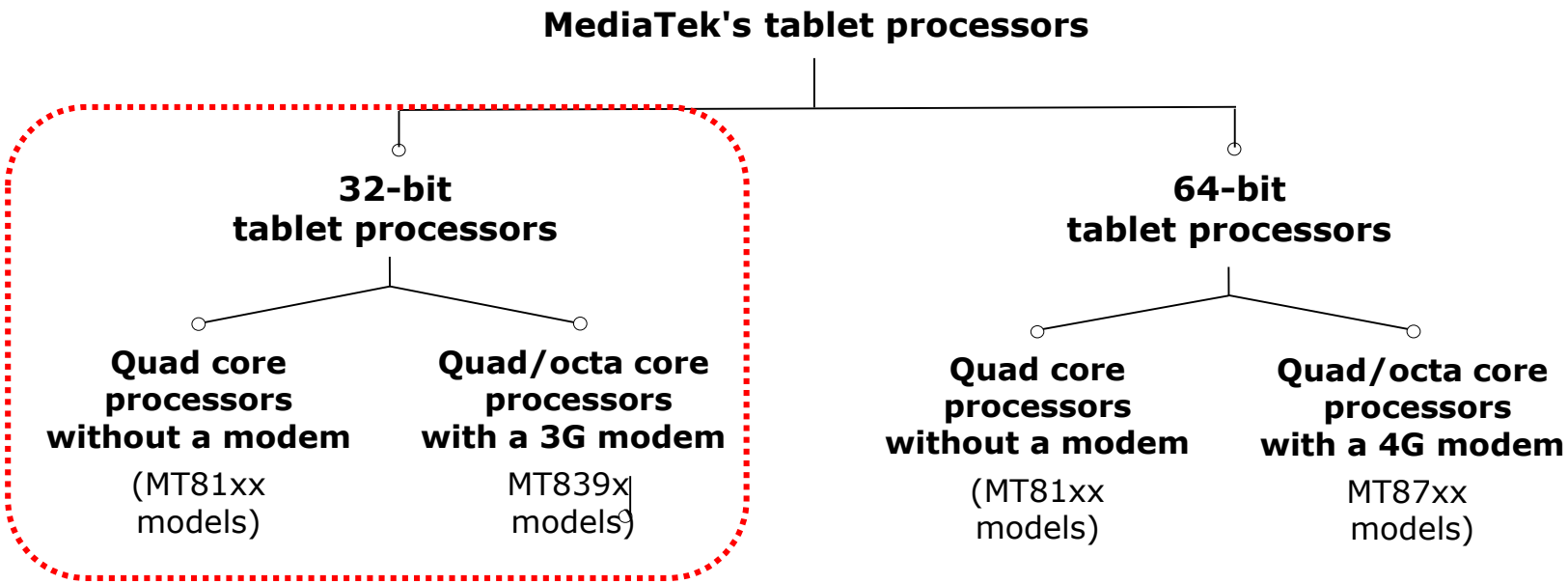
In this Section we restrict us to quad and octa core tablet processors.

Subsequently, first we give an overview of MediaTek's 32-bit quad- and octa core tablet application processors followed by their 64-bit companions.



3.2 MediaTek’s 32-bit tablet processors

3.2 MediaTek’s 32-bit tablet processors



3.2 MediaTek's 32-bit quad- and octa core tablet processors [12]

Model Number	Intro.	CPU	Techn.	GPU	Memory techn. up to	Conectivity	Utilising devices
MT8382	1H/2014	1.3 GHz quad-core Cortex-A7	28 nm	Mali-400 MP2 @ 500 MHz	LPDDR2/LP DDR3	Rel. 8 HSPA+/ TD-SCDMA, WiFi, GPS Bluetooth	• Acer Iconia A1-713 • Lenovo Tab A7-50 3G
MT8125	1H/2013	1.2 GHz quad-core Cortex-A7	28 nm	PowerVR SGX544MP1 @ 256 MHz	32-bit LPDDR2/ DDR3L	WiFi, Bluetooth	• ASUS MeMO Pad HD 7
MT8389/ MT8389T	1H/2013	1.2/1.5 GHz quad-core Cortex-A7	28 nm	PowerVR SGX544 @ 286/357 MHz	32-bit LPDDR2/ DDR3L	3G/HSPA+, 2G/ EDGE, WiFi, GPS, Bluetooth, FM	• Lenovo IdeaTab S6000H
MT8121	2H/2013	1.3 GHz quad-core Cortex-A7	28 nm	PowerVR SGX544 @ 156 MHz	LPDDR2/ LPDDR3	WiFi, GPS Bluetooth	• Lenovo A8-50 WiFi, • Lenovo A10-70 WiFi
MT8127	2014	1.3 GHz quad-core Cortex-A7	28 nm	Mali-450 MP4 @ 600 MHz	LPDDR2 /LPDDR3 667 MT/s	WiFi, GPS, Bluetooth, FM	• ALCATEL ONETOUCH • Cube U25GT • DigiLand DL1010Q
MT8135	07/2013	1.2 GHz dual A7 + 1.7 GHz dual A15	28 nm	PowerVR G6200 @ 450 MHz	LPDDR3-1333	WiFi, GPS, Bluetooth, FM	• (CorePilot introduced)
MT8392	1H/2014	up to 2.0 GHz octa-core Cortex-A7	28 nm	Mali-450 MP4 @ 700 MHz	LPDDR2 /LPDDR3 667 MT/s	3G/HSPA+, GPS, WiFi, FM, Bluetooth	• Cube Talk9X U65GT

3.2 MediaTek's 32-bit tablet processors (3)

We note that

- all processors - except of the MT8135 - are symmetrical multicores.
- The quad core MT8135 is built up in the big.LITTLE configuration.

  It is the first big.LITTLE configuration with inclusive core switching (GTS) in the world.

  Subsequently, we give some more details of the MT8135.
- The MT8392 is the world's first true (32-bit) octa-core tablet platform meaning that at the same time even all eight cores may be active.

  Also we will recite performance scores relating to the MT8392.

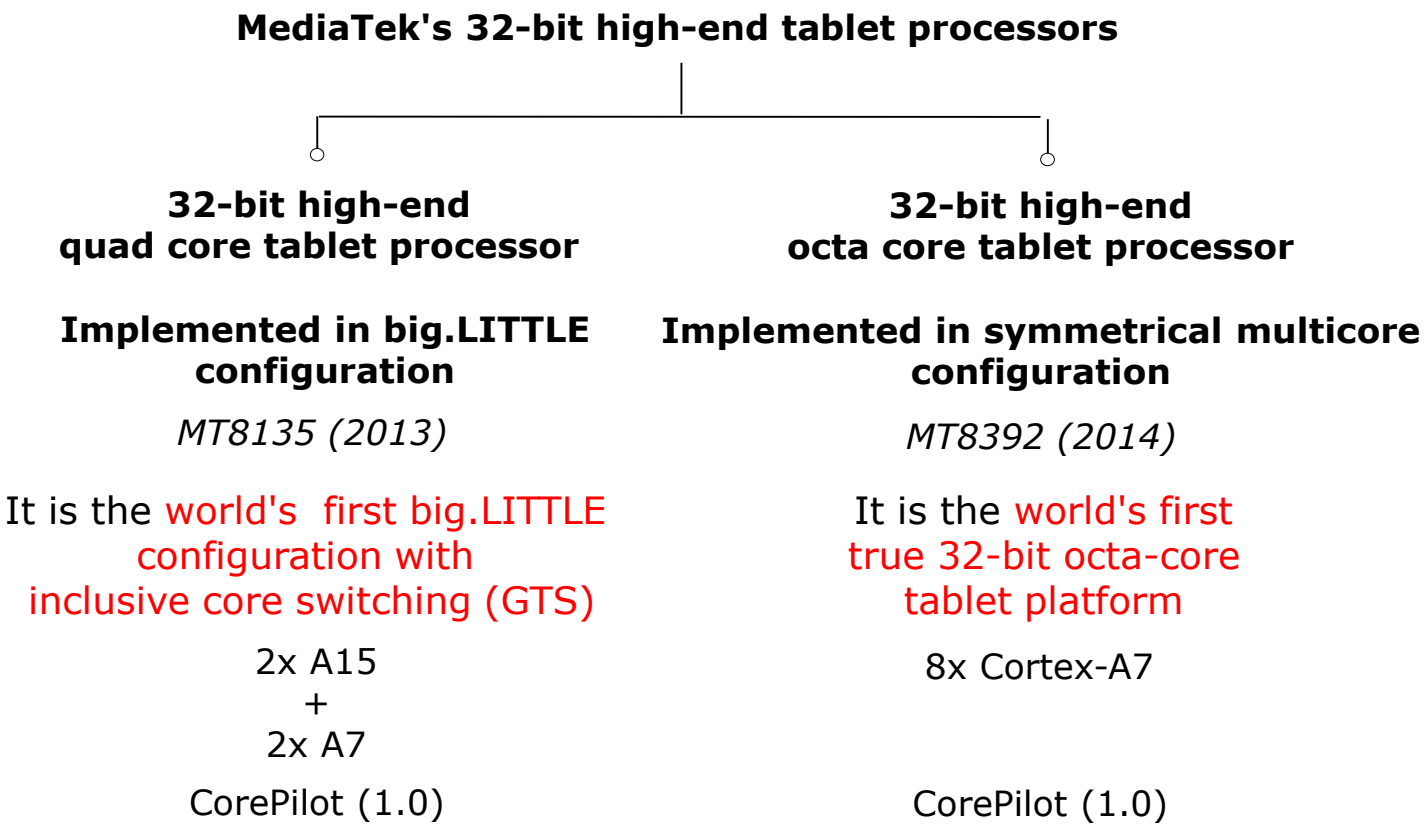
3.2 MediaTek's 32-bit tablet processors (4)

MediaTek's 32-bit high-end tablet processors

MediaTek launched only two 32-bit high-end tablet processors:

a) the quad core MT8135 implemented as a big.LITTLE multicore SOC including dual high-end A15 and dual A7 cores and

b) the octa core MT8392 implemented as a symmetrical multicore with A7 cores.



3.2 MediaTek's 32-bit tablet processors (5)

Example 1: MediaTek's only 32-bit high-end tablet SOC in big.LITTLE configuration: the MT8135

- The MT8135 is designed for android tablets.
- It is the first big.LITTLE configuration with inclusive core switching (HPM or GTS) in the world.
- Announced in 7/2013, launched in 8/2013.
- It is a quad-core SOC in a big.LITTLE configuration consisting of two clusters, as seen below.

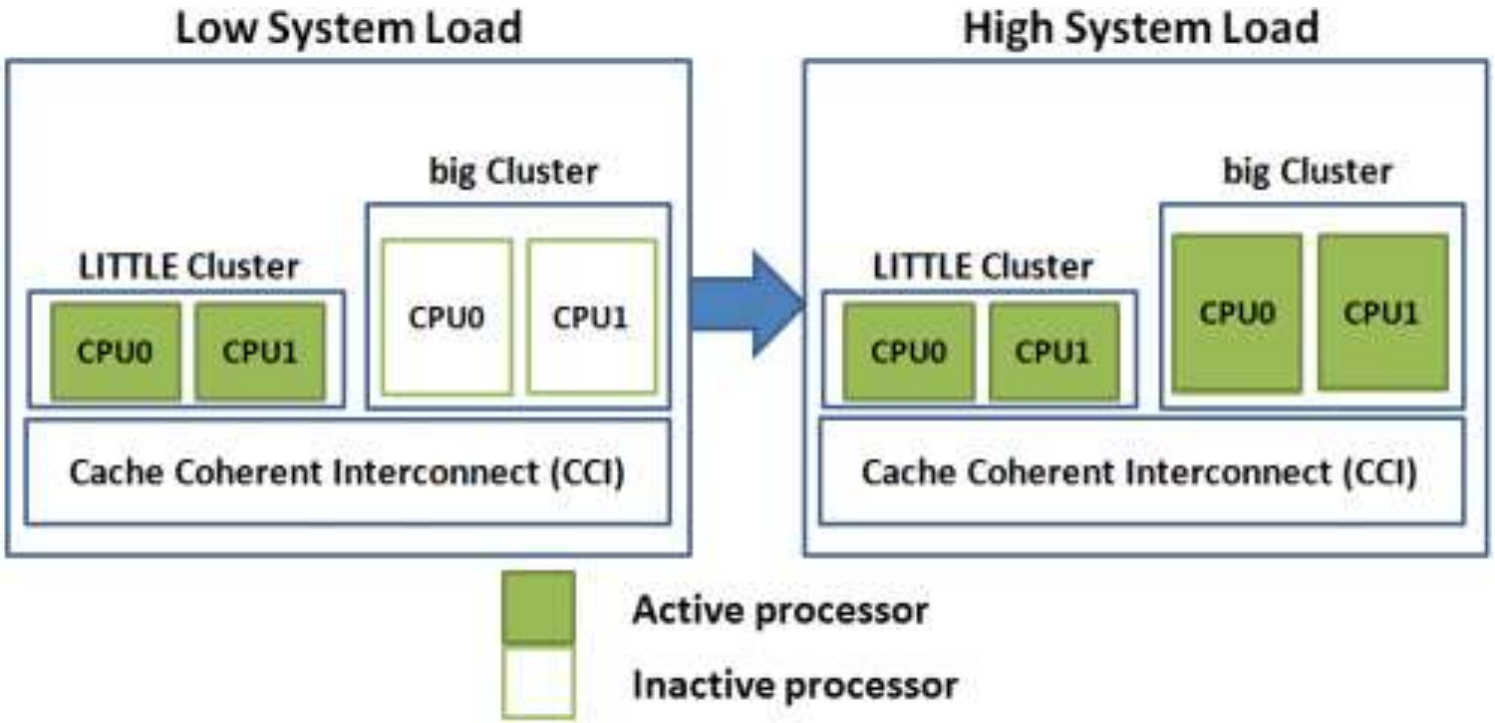
Key features of MediaTek's MT8135 32-bit tablet processor

Model Number	Intro.	CPU	Techn.	GPU	Memory techn. up to	Conectivity	Utilising devices
MT8135	07/2013	1.2 GHz dual A7 + 1.7 GHz dual A15	28 nm	PowerVR G6200 @ 450 MHz	LPDDR3-1333	WiFi, GPS, Bluetooth, FM	• (CorePilot introduced)

- The MT8135 runs under MediaTek's proprietary CorePilot software that implements GTS and allows activating all four cores at the same time, as shown in the next Figure.

3.2 MediaTek's 32-bit tablet processors (6)

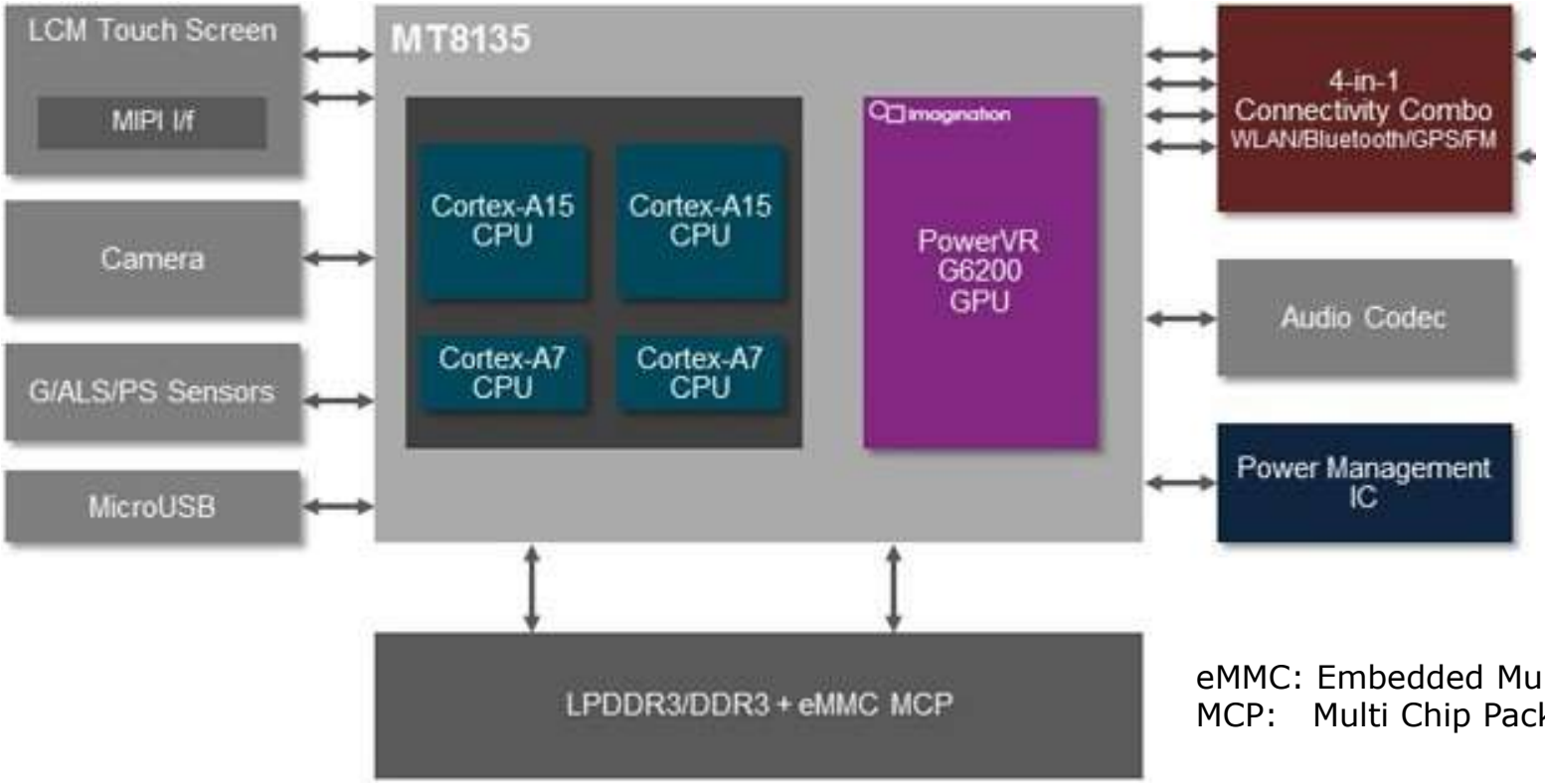
Principle of operation of the MT8135 [13]



Note that unlike the original cluster switching implementation where only one cluster can operate at any given time now also all cores can be active at the same time for high system loads.

3.2 MediaTek's 32-bit tablet processors (7)

Block diagram of the MT8135 [14]



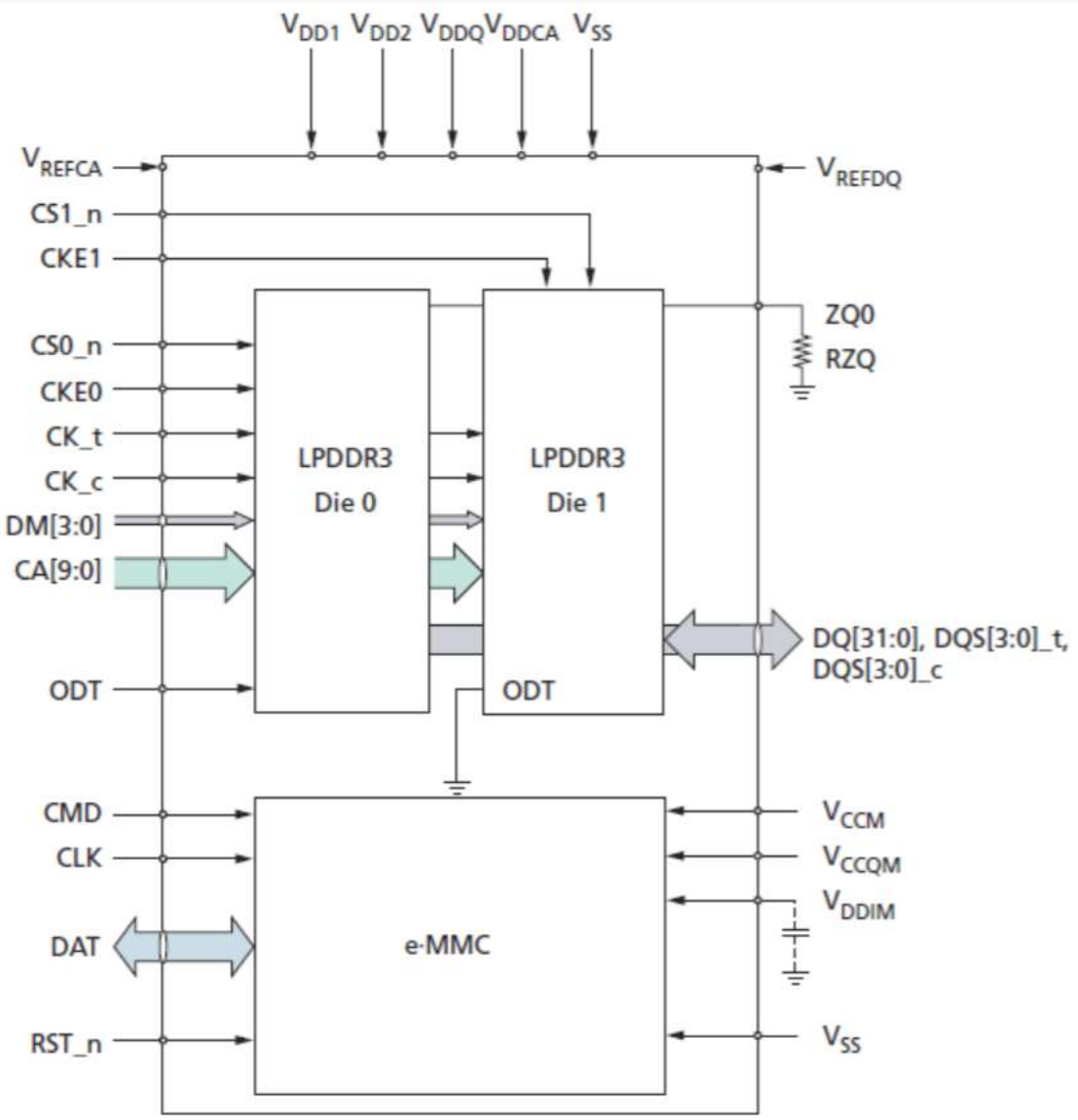
eMMC: Embedded MultiMedia Card
MCP: Multi Chip Package

Note that the MT8135 includes also a GPU, the PowerVR G6200, but does not provide mobile connectivity .

Memory is provided by an MCP package that includes both LPDDR3/DDR3 and eMMC memory, as indicated in the next Figure.

3.2 MediaTek's 32-bit tablet processors (8)

Assumed layout of the MCP providing both LPDDR3 and eMMC memory [46]

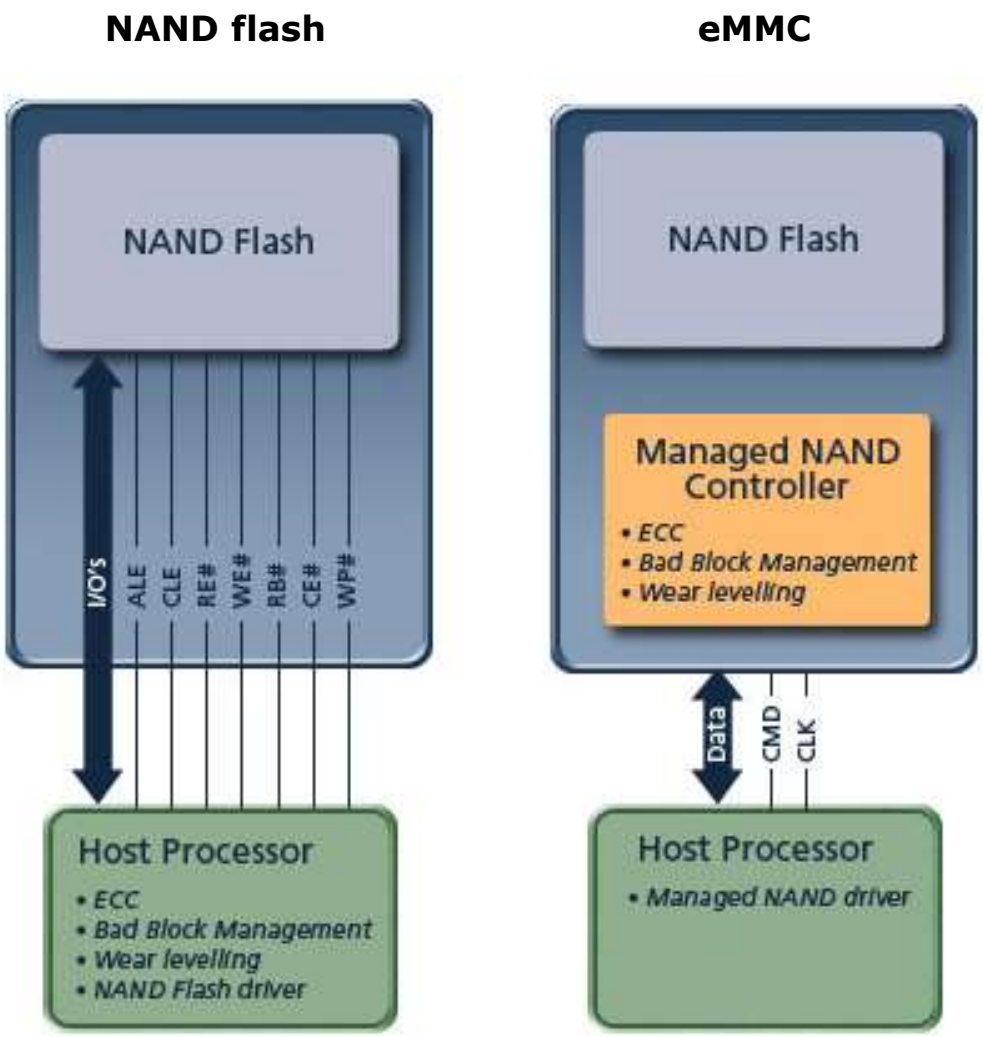


3.2 MediaTek's 32-bit tablet processors (9)

eMMC (Embedded Multi Media Card) [15]

- Recently, portable consumer electronics products, like smart phones or tablets typically store their data on flash memory.
- Using a flash memory needs a dedicated controller to manage the reading and writing of data, ECC etc, the controller is driven by the host processor.
- In the past the controller was part of the platform.
- eMMC refers to a solution when the memory package includes both the flash memory and the flash memory controller integrated on the same silicon die, as the next Figure shows.

eMMC vs. traditional flash memory implementation [16]



Example for eMMC

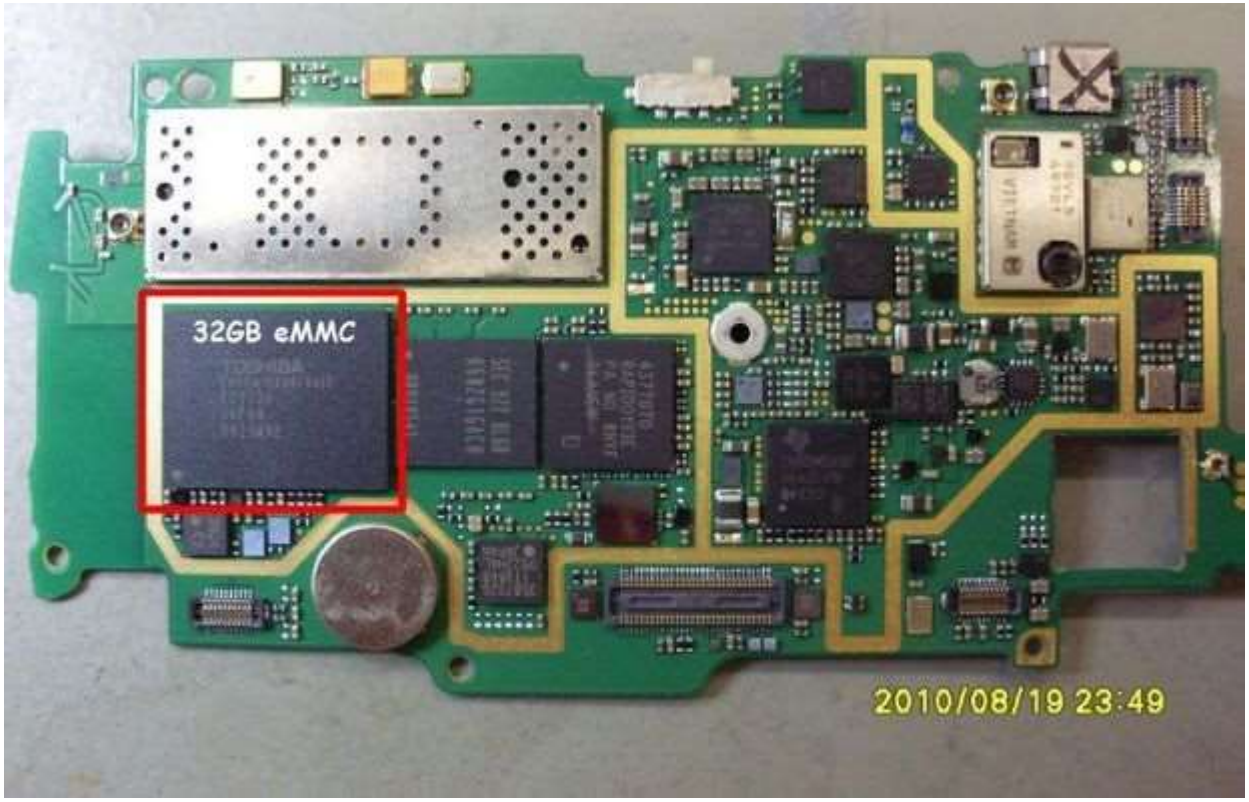


Figure: 32 GB eMMC on a Nokia N97 board [17]

eMMC standards

The standardisation body JEDEC (Joint Electron Device Engineering Council) works out and maintains standards for eMMC.

Remark

The widely accepted standard for eMMC is JESD84-A441: Embedded MultiMediaCard (e•MMC) Product Standard v4.5, JEDEC, June 2011.

3.2 MediaTek's 32-bit tablet processors (13)

Key benefits of integrating the flash memory and its controller

- It releves the host processor from low-level flash memory management.
- it also simplifies the flash memory interface design and reduces the time-to-market.

3.2 MediaTek's 32-bit tablet processors (14)

Example 2: MediaTek's 32-bit high-end octa core tablet processor operating in symmetrical multicore configuration: the MT8392

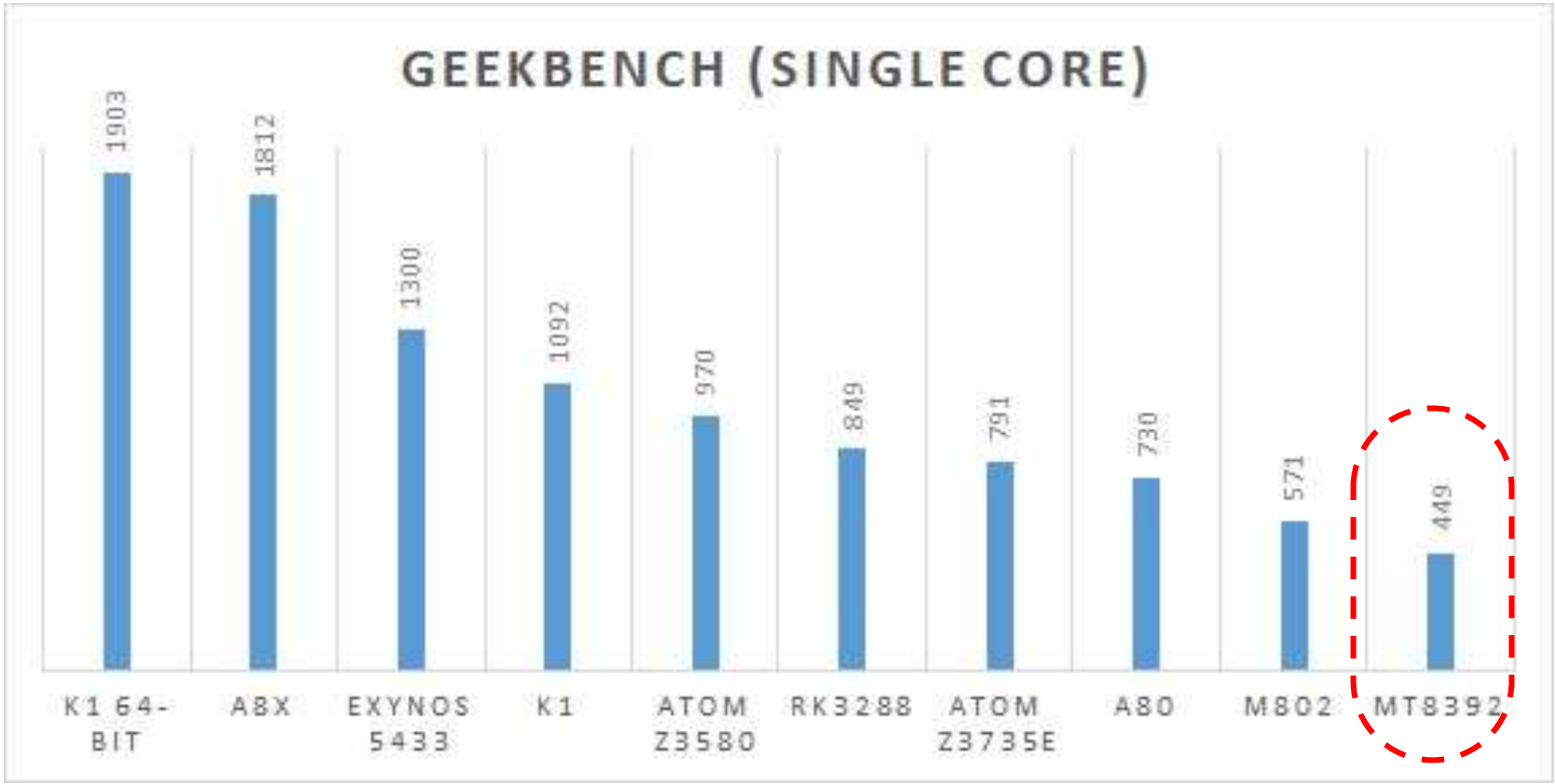
Key features of MediaTek's MT8392 32-bit tablet processor

Model Number	Intro.	CPU	Techn.	GPU	Memory techn. up to	Conectivity	Utilising devices
MT8392	1H/2014	up to 2.0 GHz octa-core Cortex-A7	28 nm	Mali-450 MP4 @ 700 MHz	LPDDR2 /LPDDR3 667 MT/s	3G/HSPA+, GPS, WiFi, FM, Bluetooth	• Cube Talk9X U65GT

- It is the world's first true 32-bit octa-core tablet platform.
  True octa core means that all cores may operate at the same time.
- The MT8392 makes use of CorePilot for scheduling (see next Section).

3.2 MediaTek's 32-bit tablet processors (15)

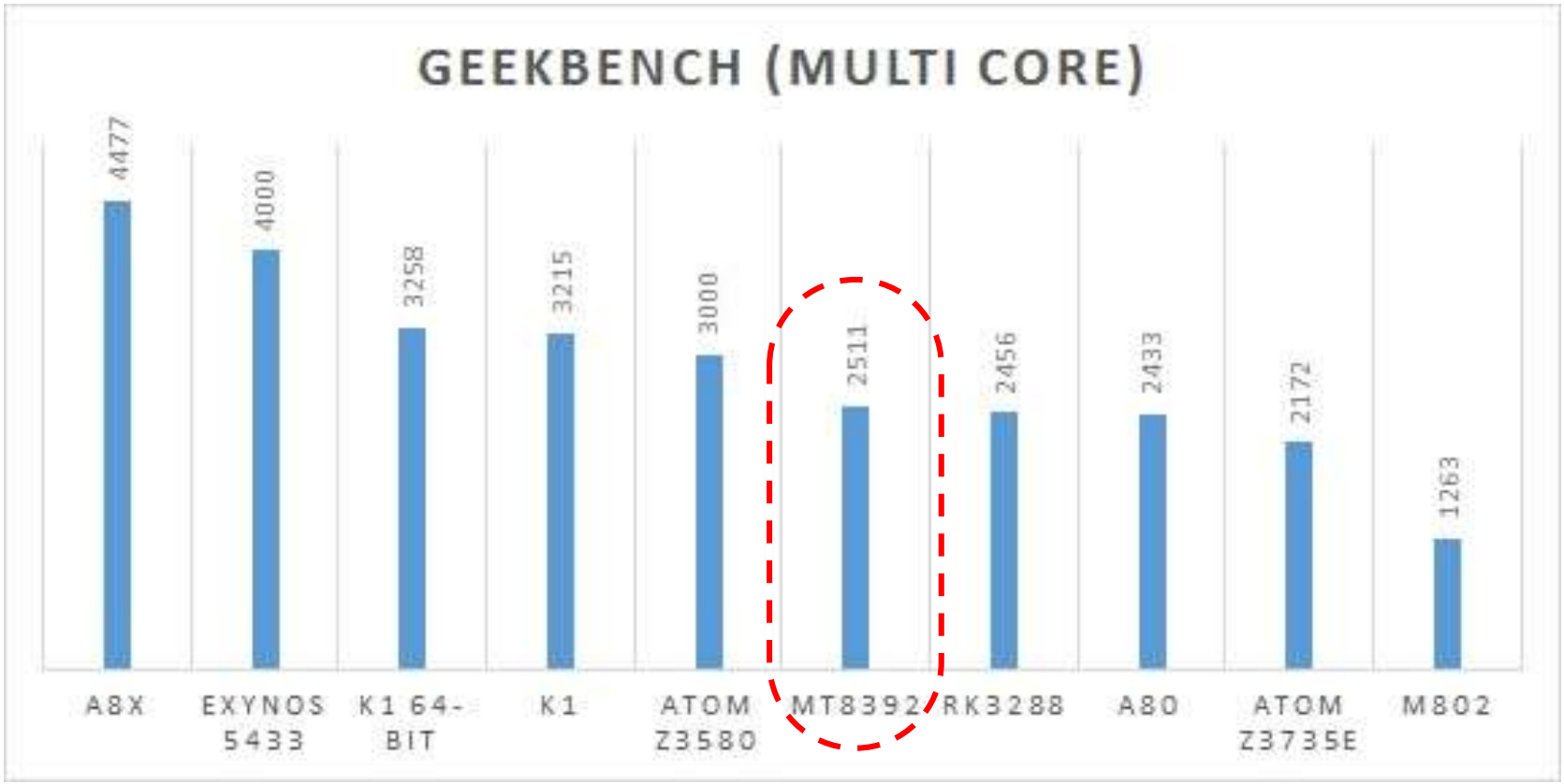
Comparing Geekbench 3 single core performance of MediaTek's 32-bit high-end octa core MT8392 tablet platform with competing designs [18]



Geekbench 3 is Primate Labs' cross-platform processor benchmark that simulates real-world scenarios. It has new workloads and a new scoring system that separates single-core and multi-core performance.

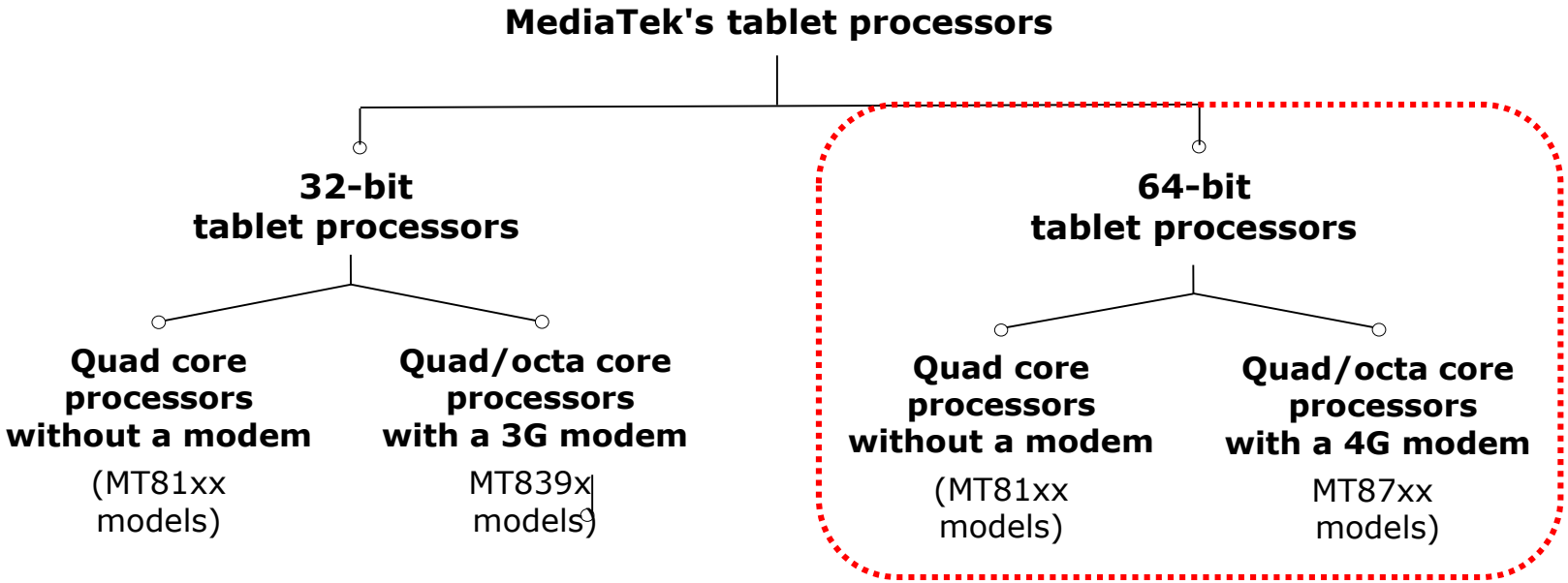
3.2 MediaTek's 32-bit tablet processors (16)

Comparing Geekbench 3 multicore performance of MediaTek's 32-bit high-end octa core MT8392 tablet platform with competing designs [18]



3.3 MediaTek’s 64-bit tablet processors

3.3 MediaTek’s 64-bit tablet processors



3.3 MediaTek's 64-bit tablet processors (2)

MediaTek's 64-bit quad core tablet processors [12]

Model No.	Intro.	Techn.	CPU	L2/core	GPU	Memory techn. Up to	Wireless radio technologies	Utilising devices
MT8161	Q4/2014	28 nm	4x 1.5 GHz Cortex-A53	½ MB L2	Mali-T760 MP2 @ 500 MHz	800 Mbps LPDDR3 (6.4 GB/s)	WiFi, Bluetooth, FM, GPS	Lenovo Tab 2 A8
MT8163	Q2/2015	28 nm	4x 1.3 GHz Cortex-A53	½ MB L2	Mali-T760 MP2 @ 520 MHz	666 Mbps LPDDR3 (5.3 GB/s	WiFi, Bluetooth, FM, GPS	Acer B3-A20-K8UH Asus ZenPad 10 Amazon Fire HD
MT8173	Q1/2015	28 nm	2x 2.0 GHz A72+ 4x 1.3 GHz A53	½ MB L2	PowerVR GX6250 @ 600 MHz	933 Mbps LPDDR3 (7.5 GB/s	WiFi, Bluetooth, FM, GPS	
MT8176	Q1/2016	28 NM	2x 2.0 GHz A72+ 4x 1.6 GHz A53	½ MB L2	PowerVR GX6250 @ 600 MHz	933 Mbps LPDDR3 (7.5 GB/s)	WiFi, Bluetooth, FM, GPS	Xiaomi Mi Pad 3 Asus ZenPad 3S 10 Acer Iconia One 7
MT8732	Q4/2014	28 nm	4x 1.5 GHz Cortex-A53	½ MB L2	Mali-T760 MP2 @ 500 MHz	800 Mbps LPDDR3 (6.4 GB/s)	LTE Cat 4 (4G/3G/2G) WiFi, Bluetooth. FM, GPS	
MT8735	Q2/2015	28 nm	4x 1.3 GHz Cortex-A53	½ MB L2	Mali-T720 MP2 @ 700 MHz?	640 Mbps LPDDR3 (4.5 GB/s)	LTE Cat 4 (4G/3G/2G) WiFi, Bluetooth. FM, GPS	

3.3 MediaTek's 64-bit tablet processors (3)

MediaTek's 64-bit octa core tablet processors [12]

Model No.	Intro.	Techn.	CPU	L2/core	GPU	Memory techn. Up to	Wireless radio technologies	Utilising devices
MT8752	Q4/2014	28 nm	8x 1.7 GHz Cortex-A53	½ MB L2	Mali-T760 MP2 @ 500 MHz	800 Mbps LPDDR3 (6.4 GB/s)	LTE Cat 4 (4G/3G/2G) WiFi, Blootooth, FM, GPS	Cube Talk T7 4G
MT8783	2015	28 nm	8x 1.3 GHz Cortex-A53	½ MB L2	Mali-T720 MP2 @ 700 MHz	800 Mbps LPDDR3 (6.4 GB/s)	LTE Cat 4 (4G/3G/2G) WiFi, Blootooth, FM, GPS	Lenovo Phab2 Plus Raptor Wave 4G Cube MT8783 4G
MT8785	Q1/2017	28 nm?	8x 2.0 GHz Cortex-A53	½ MB L2	Mali-T860 MP2 @ 700 MHz	800 Mbps LPDDR3 (6.4 GB/s)	LTE Cat 6 (4G/3G/2G) WiFi, Blootooth, FM, GPS	Lenovo Phab 2 PB2-650Y

Remarks

- All quad and octa core processors are implemented as symmetrical multicores.
- They are running under MediaTek's CorePilot task scheduling software.
- MediaTek's all octa core tablet processors are high-end models.
- We point out that MediaTek's MT8752 is the world's first 64-bit octa-core LTE (cat. 4) tablet SOC.

3.3 MediaTek’s 64-bit tablet processors (4)

- Remark
- At writing these slides MediaTek did not yet newer tablet processors.
- Presumably, this is due to lower than expected selling figures.

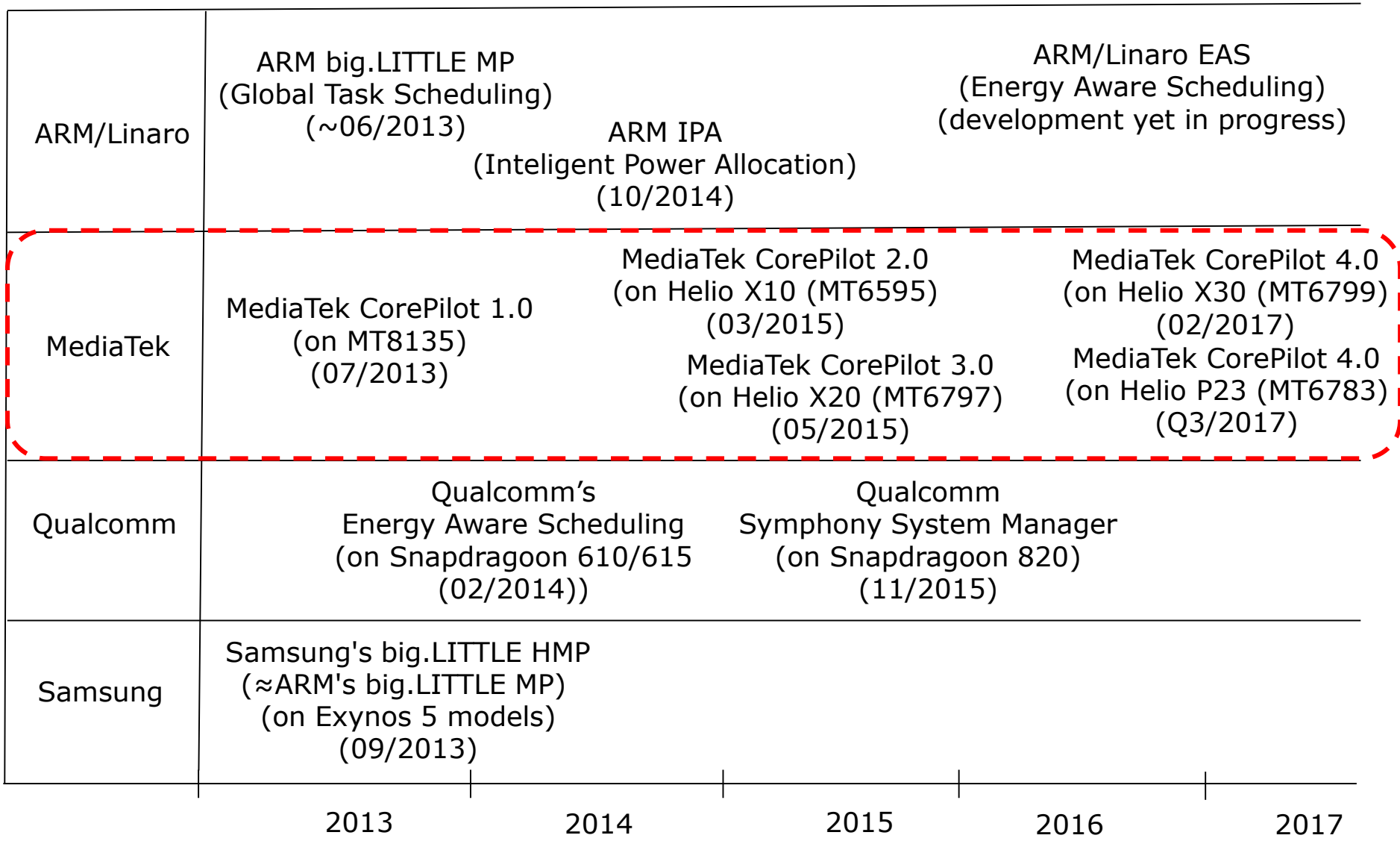
4. MediaTek’s CorePilot task scheduler

- 4.1 Overview
- 4.2 CorePilot 1.0
- 4.3 CorePilot 2.0
- 4.4 CorePilot 3.0
- 4.5 CorePilot 4.0

4.1 Overview

4.1 Overview

MediaTek's CorePilot vs. similar control software of the competition

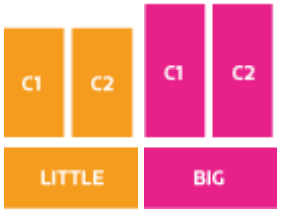


4.1 Overview (2)

Overview of subsequent CorePilot versions (Based on 28)

Symmetric Multiprocessing

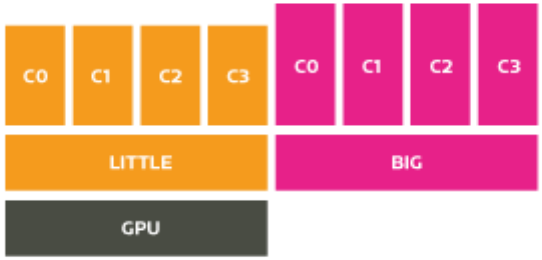
big.LITTLE processing



CorePilot™ 1.0

Quad core or octa core with big.LITTLE, or octa core SMP with Global Task scheduling (GTS)

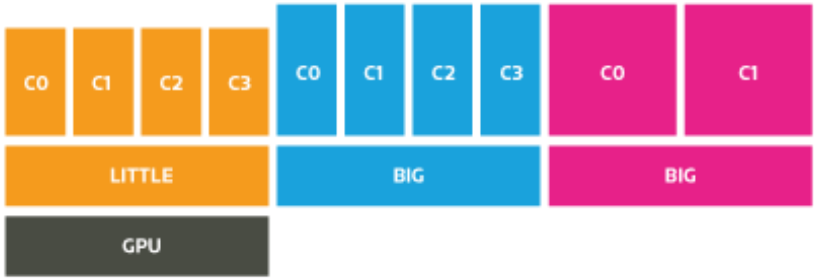
Heterogeneous Computing



CorePilot™ 2.0

CPU+GPU computing

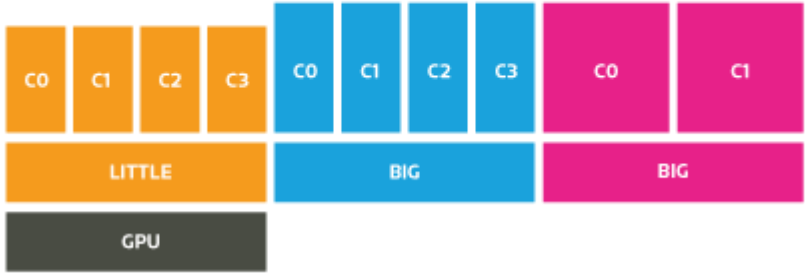
Hybrid Three-Cluster Multi-Processing



CorePilot™ 3.0

Tri-Cluster (deca core) CPU architecture

Centralized, Intelligent Task Scheduling



CorePilot™ 4.0

Thermal management
UX (User Experience) monitoring

4.2 CorePilot (1.0)

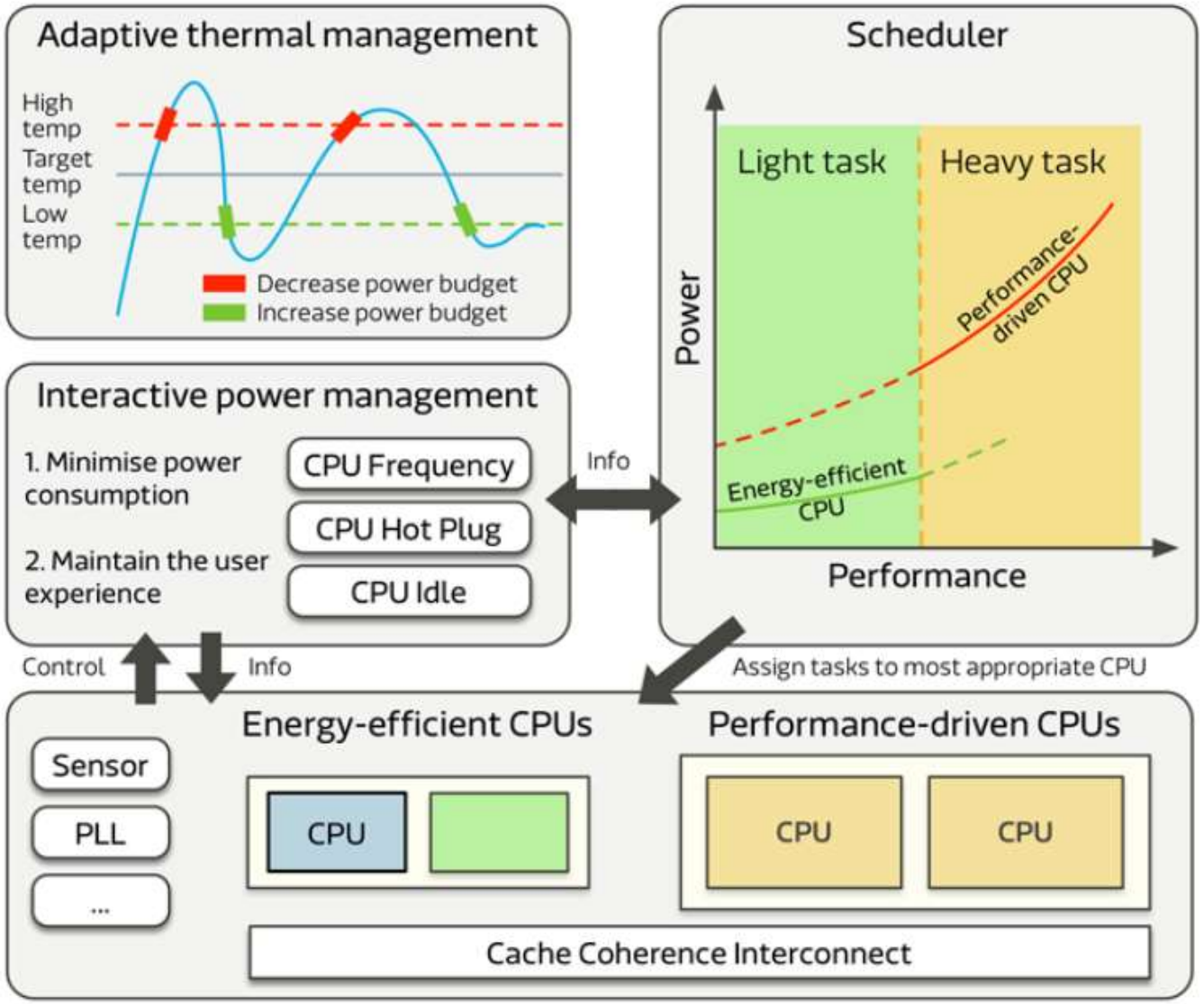
4.2 CorePilot (1.0) [14]

- It is based on the open-source GTS (Global Task Scheduling) technology, designated as big.LITTLE MP, that was developed by Linaro.

  CorePilot was introduced along with the MT8135 in 07/2013.
- It integrates thermal and power management with task scheduling and consists accordingly of the following three parts:
  - adaptive thermal management
  - interactive power management and
  - advanced scheduler algorithms,

  as indicated in the next Figure.

Overview of the operation of CorePilot 1.0 [14]



Task scheduling alternatives of heterogeneous processors [12]

	Cluster Migration	CPU Migration	Heterogeneous Multi-Processing
Switching Granularity	Cluster – low flexibility	CPU – medium flexibility	Unrestricted – high flexibility
Maximum Performance	Medium: 2x 'big'	Medium: 2x 'big'	High: 2x 'big' + 2x 'LITTLE'
Average Power Saving	Low – coarse granularity	Medium	High – fine granularity

- Heterogeneous multiprocessing (HMP, aka GTS (Global Task Scheduling)) allows the scheduler to allocate any task to any big or LITTLE core.
- It is inherently superior to cluster or CPU migration.
- MediaTek's MT8135 tablet processor was the first on the market to employ HMP (in 07/2013).

4.2 CorePilot (1.0) (4)

a) Adaptive Thermal Management [19]

- Power, thermal and performance (PTP) detectors are placed within the CPU to sense operating conditions.
- Adaptive Thermal Management monitors sensed data and allows the device to use the available voltage margin either to increase performance or lower power consumption when possible.
- According to MediaTek this technology allows for a 23% increase in clock speed or up to 41% power savings, depending on the SoC operating conditions.

4.2 CorePilot (1.0) (5)

b) Interactive Power Management [14]

- CorePilot's Interactive Power Manager reduces the amount of power and heat generated by the cores via two main modules.
- The DVFS (Dynamic Voltage and Frequency Scaling) module automatically adjusts the frequency and voltage of cores on the fly, while the CPU Hot Plug module switches cores on and off on demand, as summarized below.

Dynamic Voltage & Frequency Scaling	Traditional symmetric multi-processors apply a unified Dynamic Voltage and Frequency Scaling (DVFS) policy to all CPUs. CorePilot's Interactive Power Management applies different DVFS policies to 'big' and 'LITTLE' cores to maximize power and thermal efficiency.
CPU Hot Plug	Interactive Power Management monitors CPU load and seamlessly switches cores on or off to save power or to increase performance. CPUs can also be switched off with non-CPU-bound tasks to reduce power consumption.

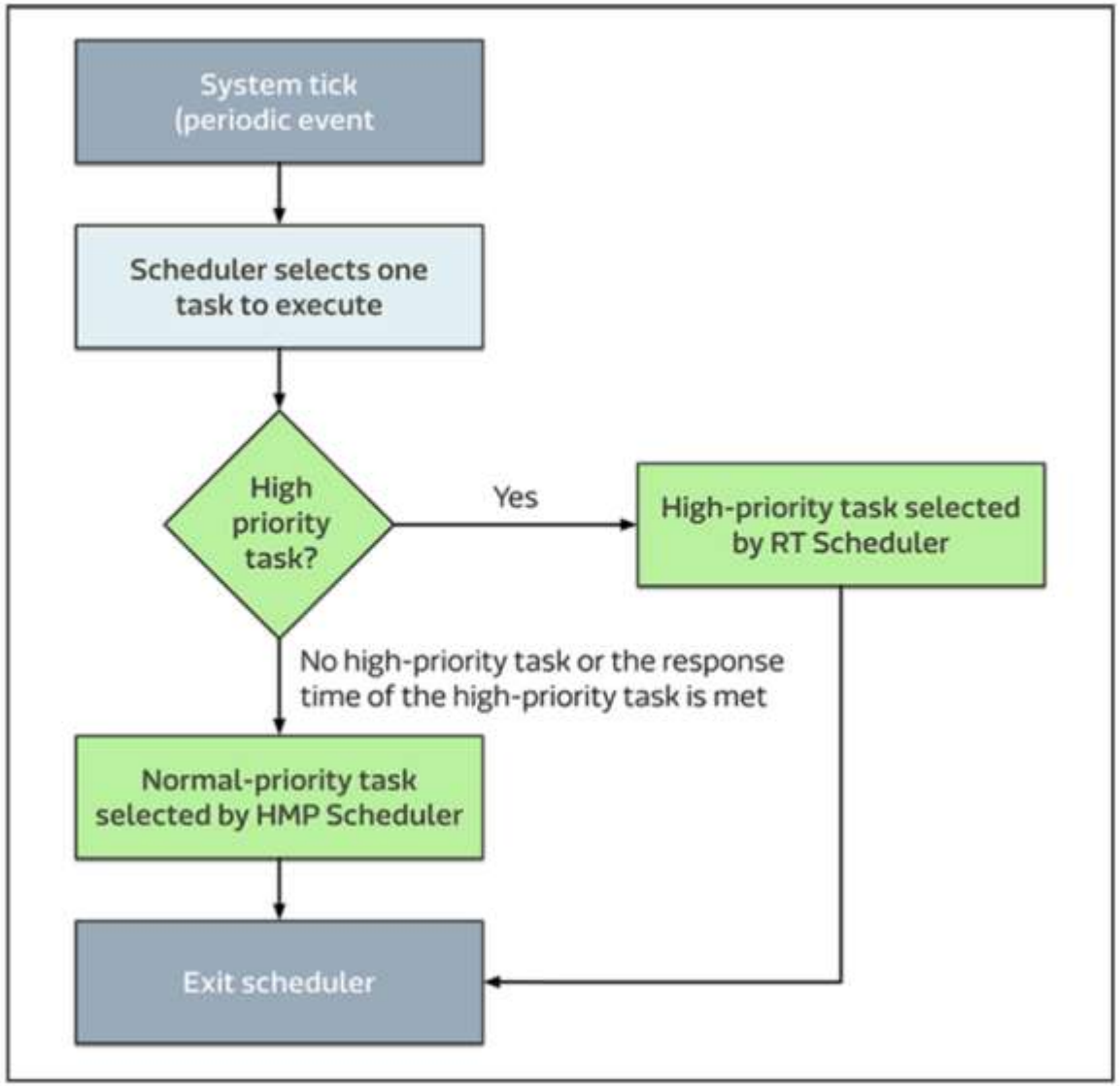
4.2 CorePilot (1.0) (6)

c) Scheduler Algorithms [14]

- With Symmetric Multi-Processing (SMP), the Completely Fair Scheduler (CFS) of the Linux kernel distributes the workload equally among CPU cores like the most common scheduling algorithms.
- In case of HMP (Heterogeneous Multi-Processing), however, CFS can cause performance degradation, since tasks do not efficiently match to CPU core capabilities.
- MediaTek's CorePilot, on the other hand, is based on a true heterogeneous compute model by using a scheduling algorithm that assigns tasks to two different schedulers, according to their priority — the Heterogeneous Multi-Processing (HMP) scheduler and the Real-Time (RT) scheduler.

4.2 CorePilot (1.0) (7)

Selection of the HMP Scheduler or the RT scheduler by CorePilot (1.0) [14]



MediaTek's HMP Scheduler

It is responsible for assigning normal-priority tasks to the big.LITTLE CPU core clusters and performs four main functions, as follows.

Load tracking	By tracking the status of each task, the HMP scheduler determines which task is heavy and which task is relatively light.
CPU Capacity Estimation	The HMP Scheduler is aware of the available compute capacity of each processor in the big.LITTLE clusters, and so is able to make the most appropriate scheduling decisions.
Intelligent Load-Balancing	Load tracking and CPU capacity estimation are used in concert for rapid load balancing – assigning and reassigning tasks to performance-driven or energy-efficient CPUs, as required.
Task Packing	The HMP scheduler consolidates as many light-load tasks as possible and matches them to the most appropriate CPUs. CPUs without active tasks can then be switched off via CPU Hot Plug, or put into an idle state.

Figure: Key components of MediaTek's HPM scheduler [14]

MediaTek's RT Scheduler [14]

- The RT scheduler assigns high-priority real-time tasks that require a fast response to the big.LITTLE cluster.
- The RT scheduler has a higher priority than the HMP scheduler.
- MediaTek has modified its design such that the highest priority tasks are assigned to high performance CPU cores whereas lesser priority real-time tasks to other available CPU cores.

4.2 CorePilot (1.0) (10)

First use cases of MediaTek's CorePilot in big.LITTLE configurations

- MT8135 2xCortex-A15 + 2x Cortex-A7 (7/2013) for Android tablets
  World's first big.LITTLE chipset.
- MT6592 8x Cortex-A7 (Q4/2013) for smartphones
  World's first octa core symmetrical multicore chipset with HSPA+ connectivity.
- MT6595 4x Cortex-A17 + 4x Cortex-A7 (7/2014) for smartphones
  World's first octa core big.LITTLE 4G LTE chipset.

4.3 CorePilot 2.0

4.3 CorePilot 2.0

- Introduced along with MediaTek's first 64-bit SOC, the Helio X10 (MT6795) in 3/2015.
- It extends the scope of the scheduler also to the GPU by including the Device Fusion technology.
- With the Device Fusion technology CorePilot 2.0 decides which task will perform better on which computing device and dispatches workloads expressed in OpenCL to the suitable computing device (CPU cores or GPU) or to both types, as shown below.

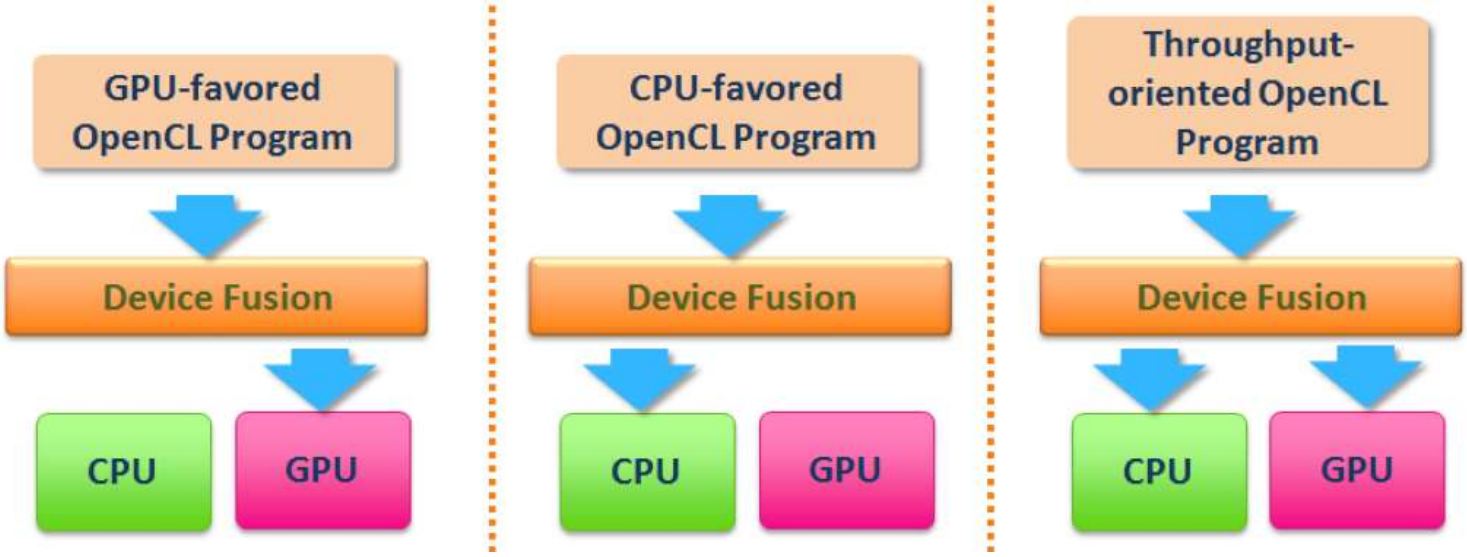


Figure: Dispatch options in the Device Fusion technology [20]

4.3 CorePilot 2.0 (2)

Expected benefits of CorePilot 2.0

MediaTek states that CorePilot promises up to 146% performance increase and up to 18 % lower energy consumption when compared to using CPU or GPU only architectures [20].

4.4 CorePilot 3.0

4.4 CorePilot 3.0 [21]

- Introduced along with MediaTek's first three cluster SOC, the Helio X20 (MT6797) in 05/2015 [22].
- CorePilot 3.0 enhances the scheduler to cope with three clusters of CPU cores as well as with the GPU while managing related power and temperature issues, as before (see the subsequent Figures).

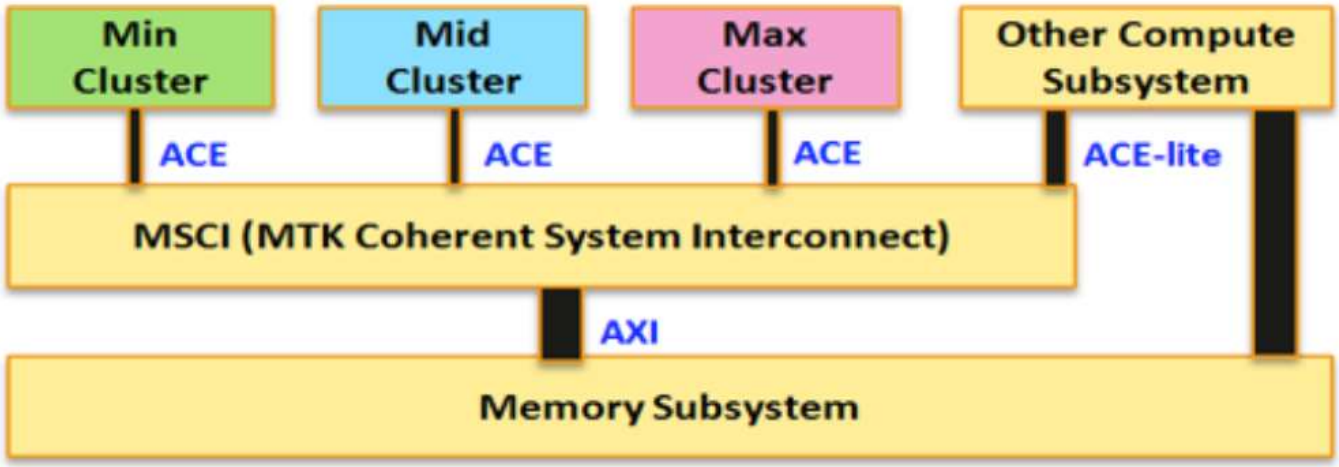
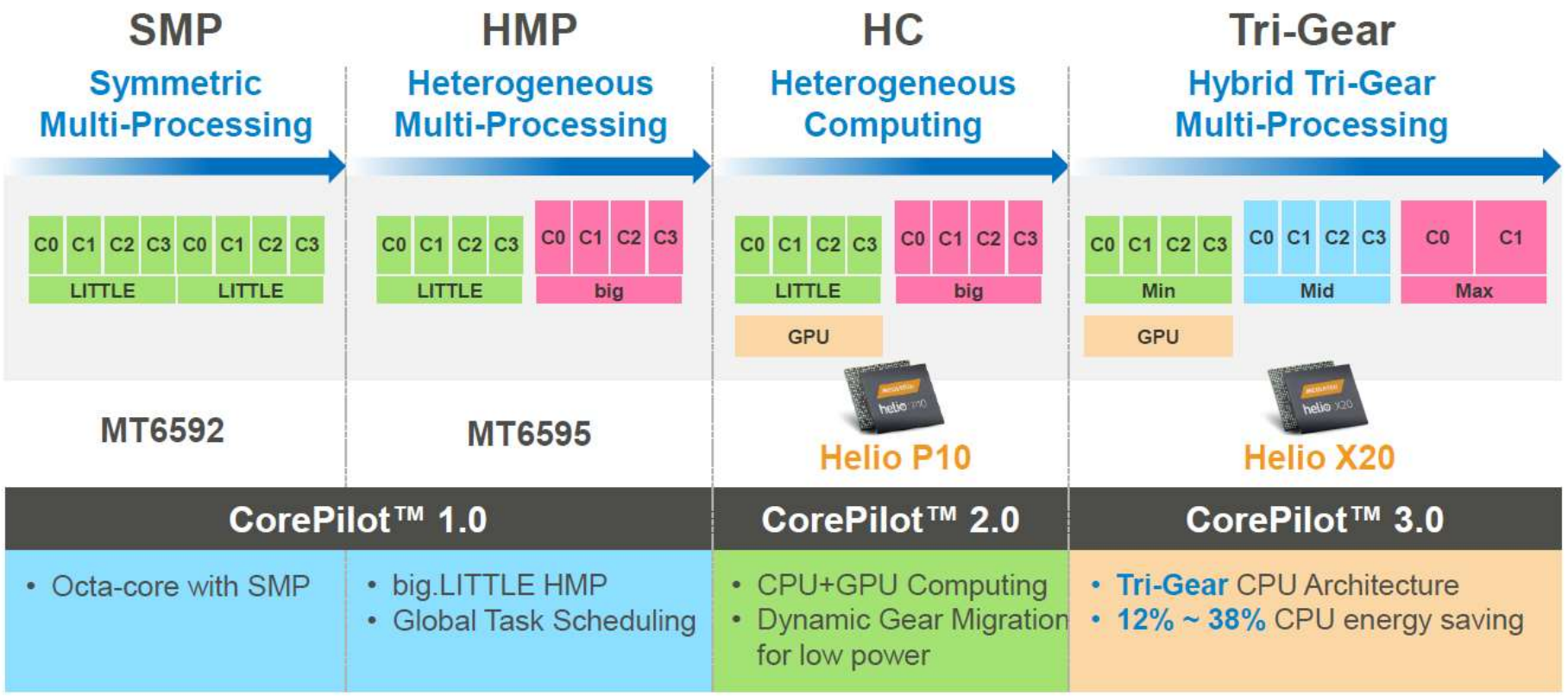


Figure: MediaTek's three cluster big.LITTLE architecture [21]

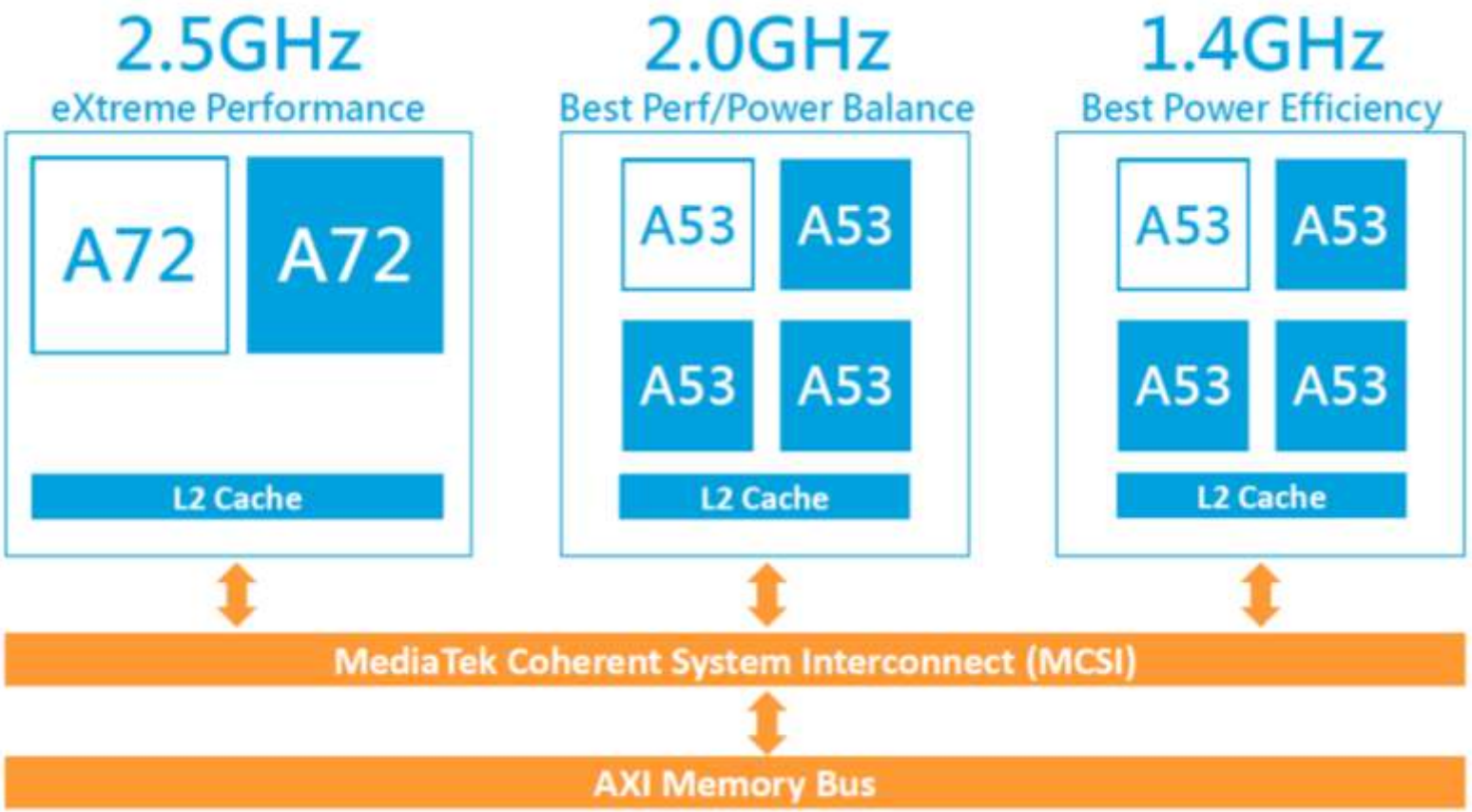
Evolution of CorePilot (up to CorePilot 3.0) [29]



4.4 CorePilot 3.0 (3)

First implementation of MediaTek's 10 core (deka core) processor (the Helio X20 (MT6797)) [23]

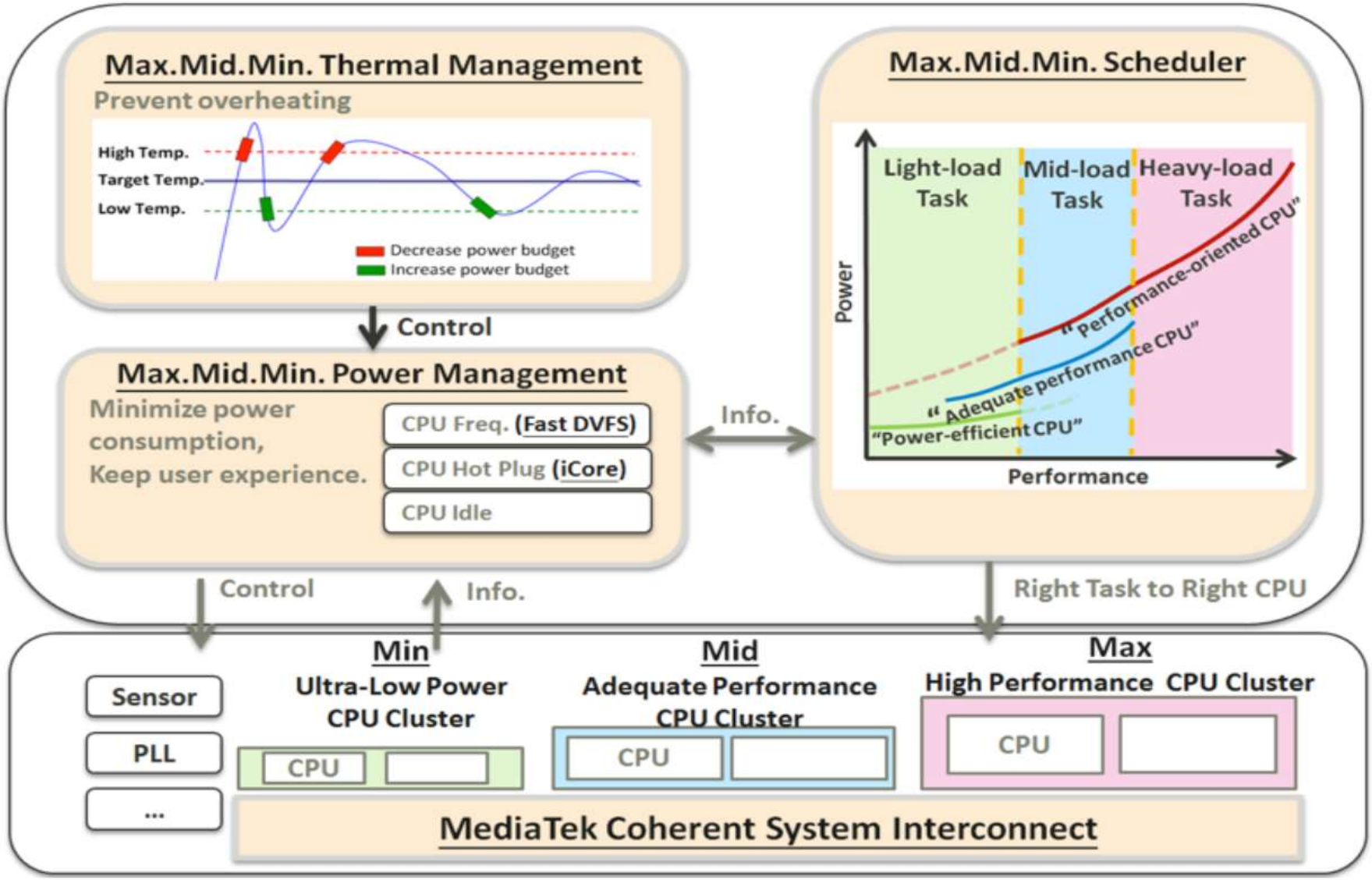
Announced in 05/2015, first apppearance in smartphones in Q4/2015.



Introducing the MediaTek Coherent System Interconnect (MCSI)

Along with the Helio X20 MediaTek introduced a proprietary system interconnect dubbed MCSI (MediaTek Coherent System Interconnect), see the Figure before.

Block diagram of CorePilot 3.0 [21]



4.4 CorePilot 3.0 (6)

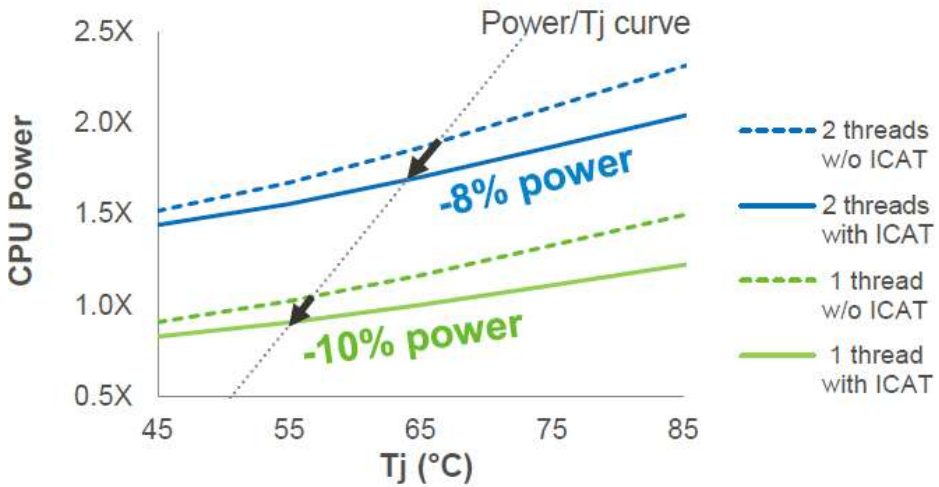
Principle of operation of CorePilot 3.0 [21]

- CorePilot 3.0 periodically calculates the allowable power budget of the SOC components based on temperature data and form factor (e.g. smartphone) heat up conditions and allocates it to the CPU cores available in three clusters and the GPU in a similar way, as before.
- In addition, thermal management prevents temperature spikes by proactively predicting temperature-rise bursts and limiting the temperature-rise speed.
- Furthermore, CorePilot 3.0 introduces the Fast DVFS technology by increasing the sampling rate up to 40 times.

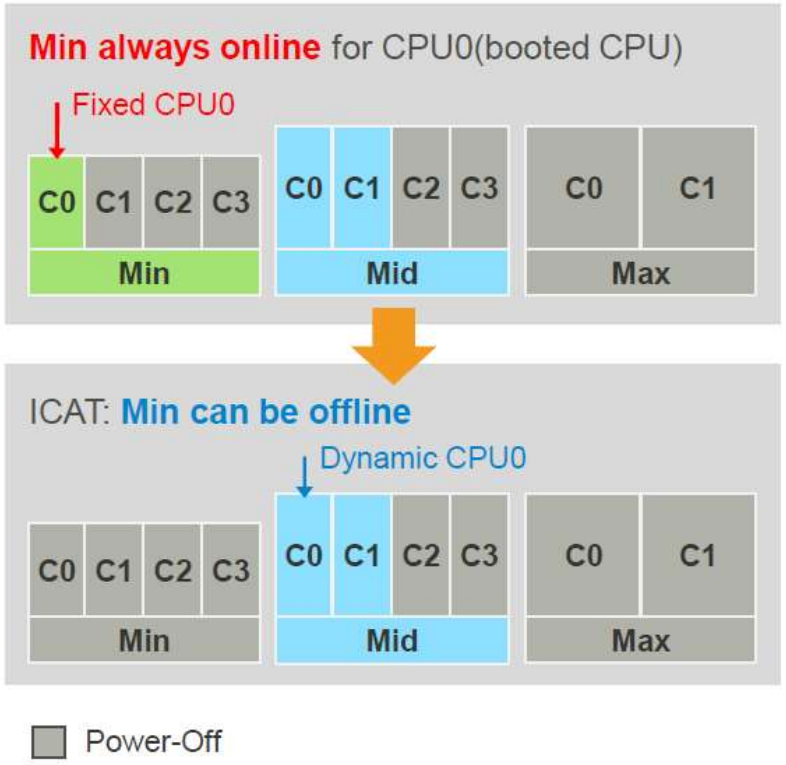
Intelligent Core Activation Technology (ICAT) [29]

ICAT assigns CPU0 dynamically

- Min gear can be off by task migration
- **8%~10%** CPU power saved for medium load



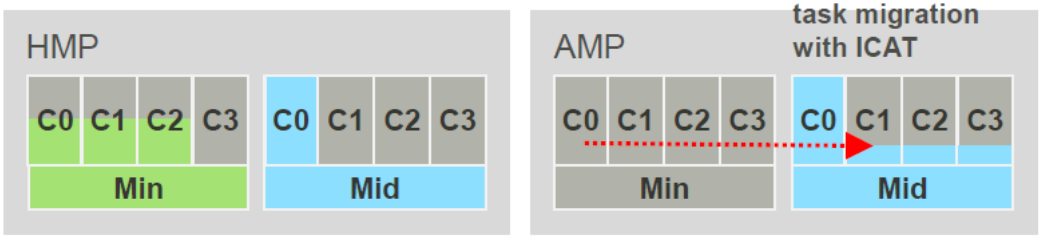
** Power is relative to 1 thread with ICAT at 65℃*



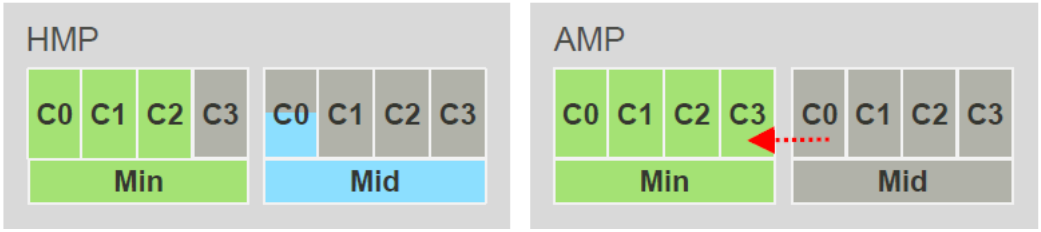
Asymmetric Multi-Processing (AMP) with ICAT [29]

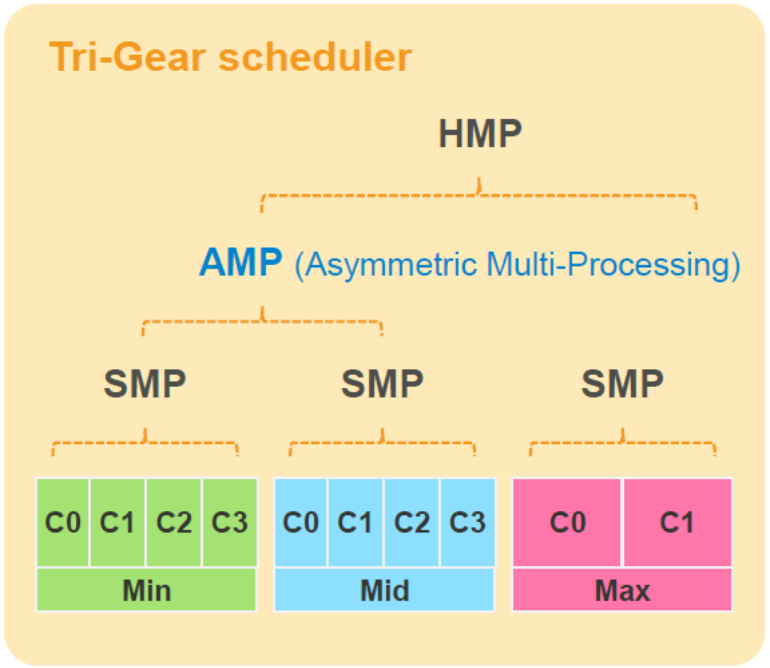
AMP: enhanced HMP with dynamic gear operation for power saving

- Packing tasks to **Mid** for sustainable performance



- Packing tasks to **Min** for low power





Instant huge core activation [21]

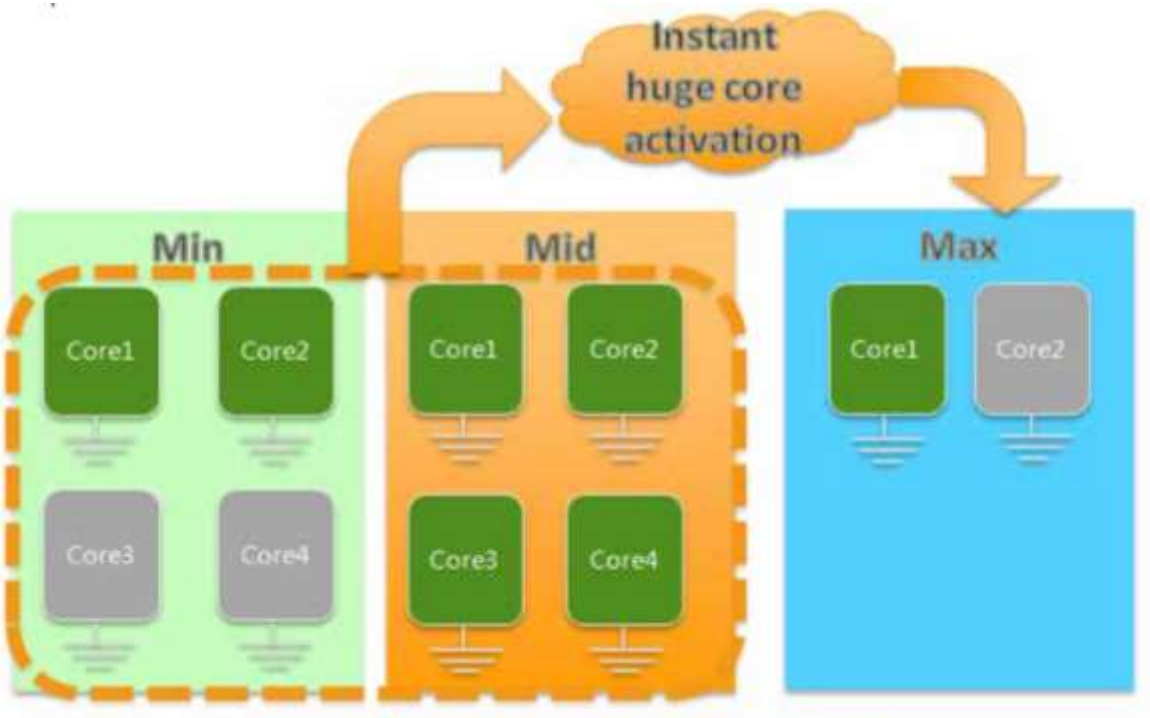


Figure 21 Instant Max CPUs Activation Example

The Fast DVFS technology

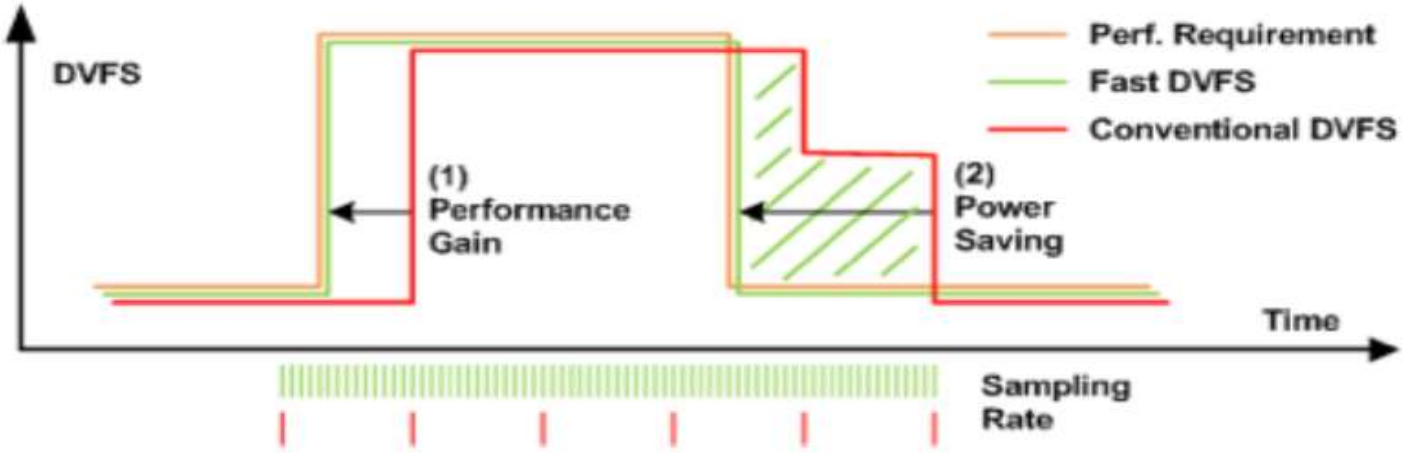


Figure: Benefits of the Fast DVFS technology [21]

Fast DVFS technology more rapidly increases clock frequency if needed to execute higher workload - providing better responsiveness, and more swiftly reduces clock frequency - if workload decreases - that results in power saving, as the above figure demonstrates.

4.5 CorePilot 4.0

4.5 CorePilot 4.0 [27]

- Announced to run on MediaTek's 10 nm Helio X30 (MT6799) in 02/2017.
- It is expected to deliver up to 25 % more power saving vs. CorePilot 3.0.
- Main enhancements over Core Pilot 3.0 are:

  including
  - thermal management and
  - user experience monitoring

  into task scheduling.

- Including thermal management into scheduling ensures that the SoC is always operating within optimal temperature ranges.
- Monitoring user experience (UX) means that the system continuously monitors decisive parameters of user experience, such as actual frame rate or activity.

  In this way task scheduling can be optimized to provide a specified standard of performance.

5. References

5. References (1)

[1]: Sawant N., From 10 million chipsets to 350 million: Decoding MediaTek's amazing rise, Tech2, Nov. 25 2014, http://tech.firstpost.com/news-analysis/interview-dr-finbarr-moynihan-discusses-mediateks-future-plans-india-rd-centres-expanding-verticals-242436.html

[2]: MediaTek is repositioning itself with the new MT6732 and MT6752 SoCs for the "super-mid market" just being born, plus new wearable technologies for wPANs and IoT are added for the new premium MT6595 SoC, Lazure, March 4 2014, http://lazure2.wordpress.com/2014/03/04/mediatek-is-repositioning-itself-with-the-new-mt6732-and-mt6752-socs-for-the-super-mid-market-just-being-born-plus-new-wearable-technologies-for-wpans-and-iot-are-added-for-the-new-prem/

[3]: Chipset Supplier MediaTek, Cnoem Phone, http://cnoemphone.com/industry/industry-chain/chipset-supplier-mediatek

[4]: MT6589 HSPA+ Smartphone Application Processor, Technical Brief, Sept. 26 2012, http://www.datasheet4u.com/datasheet/M/T/6/MT6589_MediaTek.pdf.html

[5]: MediaTek True Octa-Core, Position Paper, http://multicorechina.files.wordpress.com/2013/07/mediatektrueocta-corepositionpaper.pdf

[6]: MT6592 Octa-Core Smartphone Application Processor, Technical Brief, July 6 2013, http://www.datasheet4u.com/datasheet-pdf/Mediatek/MT6592/pdf.php?id=844976

[7]: Lilly P., Samsung Galaxy Note 4 Makes Cameo In AnTuTu With Strong Performance From Exynos 5433, Hot Hardware, June 23 2014, http://hothardware.com/news/samsung-galaxy-note-4-makes-cameo-in-antutu-with-strong-performance-from-exynos-5433

5. References (2)

[8]: MT6595 Octa-Core Smartphone Application Processor, Technical Brief, Dec. 31 2013

[9]: Tu F., An analysis of next-gen CPUs: MediaTek MT6732 MT6752 and MT6595, Gizmochina, June 23 2014, http://www.gizmochina.com/2014/06/23/an-analysis-of-next-gen-cpus-mediatek-mt6732-mt6752-and-mt6595/

[10]: MT6752 LTE Smartphone Application Processor, Technical Brief, Version: 1.2, June 10 2014

[11]: Antutu Chip Performance TOP 10, April 2016, May 18 2016, http://www.antutu.com/en/view.shtml?id=8235

[12]: Wikipedia, MediaTek, http://en.wikipedia.org/wiki/MediaTek

[13]: Lin T.Y., MediaTek MT8135 SoC - Heterogeneous big.LITTLE Processing for Mainstream, Aug. 7 2013, http://community.arm.com/groups/processors/blog/2013/08/07/mediatek-mt8135-soc--heterogeneous-biglittle-processing-for-mainstream

[14]: MediaTek CorePilot, Heterogeneous Multi-Processing Technology, 2013 http://cdn-cw.mediatek.com/MediaTek_CorePilot.pdf

[15]: What is eMMC?, Datalight, https://www.datalight.com/solutions/technologies/emmc/what-is-emmc

[16]: Shivram R.V., e-MMC (Embedded MultiMedia Card), Richiervs, June 13 2012, http://richiervs.blogspot.hu/2012/06/e-mmc-embedded-multimedia-card.html

[17]: 32 GB EMMC Memory Micro SD card Connection, 320 Volt, http://320volt.com/en/32-gb-emmc-bellege-sd-kart-baglantisi/

5. References (3)

[18]: Englert J., SOC Royal Rumble! iPad Air 2 vs. Nexus 9 vs. China Tablet SOCS, Mobile Droid, 2014, http://www.mobiledroid.co.uk/blog/soc-royal-rumble-ipad-air-2-vs-nexus-9-vs-china-tablet-socs/

[19]: Wang A., Lin T.Y., Ouyang S., Huang W.H., Heterogeneous multi-processing quad-core CPU and dual-GPU design for optimal performance, power, and thermal tradeoffs in a 28nm mobile application processor, ISSCC, 2014

[20]: MediaTek CorePilot 2.0, White Paper, http://cdn-cw.mediatek.com/White%20Papers/MediaTek_CorePilot%202.0_Final.pdf

[21]: MediaTek CorePilot 3.0, White Paper, 9/2015, http://cdn-cw.mediatek.com/White%20Papers/MediaTek%20CorePilot%203.0%20White%20Paper%20PDFCP3WP%200915.pdf

[22]: MediaTek Launches the MediaTek Helio X20: The World's First Mobile SoC Featuring Tri-Cluster CPU Architecture, May 12 2015, http://www.mediatek.com/en/news-events/mediatek-news/mediatek-launches-the-mediatek-helio-x20-the-worlds-first-mobile-soc-featuring-tri-cluster-cpu-architecture/

[23]: Cunningham A., MediaTek escalates the multicore madness with a 10-core smartphone SoC, Ars Technica, May 12 2015, http://arstechnica.com/gadgets/2015/05/mediatek-escalates-the-multicore-madness-with-a-10-core-smartphone-soc/

[24]: Lucic K., MediaTek's Roadmap Leaks, 20nm MT6796 To Arrive At The End Of 2015, Android Headlines, Febr. 28 2015, http://www.androidheadlines.com/2015/02/mediateks-roadmap-leaks-20nm-mt6796-arrive-end-2015.html

5. References (4)

[25]: Mediatek Smartphone SoC Roadmap Until 2015, CNX-Software, Febr. 28, 2014, http://www.cnx-software.com/2014/02/28/mediatek-smartphone-soc-roadmap-until-2015/

[26]: Frumusanu A., MediaTek at MWC 2015: A72 In Silicon, Multi-Standard Wireless Charging & More, AnandTech, March 8 2015, http://www.anandtech.com/show/9057/mediatek-at-mwc-2015-a72-already-in-silicon

[27]: MediaTek Press Release, Barcelona, Febr. 27, 2017 https://www.mediatek.com/press-room/press-releases/mediatek-announces-corepilot-4-0-technology-to-deliver-ultimate-processing-power-and-power-efficiency-to-smartphones

[28]: Mediatek Corepilot, https://www.mediatek.com/features/corepilot-evolution

[29]: Lin T.-Y.,Helio X20: The First Tri-Gear Mobile SoC with CorePilot™ 3.0 Technology, Hot Chips 28, Aug. 2016, https://www.hotchips.org/wp-content/uploads/hc_archives/hc28/HC28.22-Monday-Epub/HC28.22.20-Moble-Epub/HC28.22.210-Helio-TsungYaoLin-MediaTek-v2.pdf

[30]: Joel, Mediatek Launches Helio P60 At An Event In Beijing, Mtknews, GizmoChina, 15 03. 2018, https://www.gizmochina.com/2018/03/15/mediatek-launches-helio-p60-at-an-event-in-beijing/

[31]: Frumusanu A., MediaTek Announces New Premium Helio P60 SoC, 03/01, 2018, AnandTech, https://www.anandtech.com/show/12451/mediatek-announces-new-premium-helio-p60-soc

[32]: Yoshida J., MWC: MediaTek Aims for Upper Midrange with AI, EE Times, Febr. 22, 2018, https://www.eetindia.co.in/news/article/18022704-mwc-mediatek-aims-for-upper-midrange-with-ai

5. References (5)

[33]: Lee Y.-L. et al., Techology trend of edge AI, Proc. **2018 International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 6-19 April 2018,** https://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=8370612

[34]: Vision DSPs for Imaging and Vision, Cadence, https://ip.cadence.com/vision

[35]: Increasing Processor Computational Performance with More Instruction Parallelism, Cadence, Oct. 2015, https://ip.cadence.com/uploads/927/TIP_WP_FLIX_FINAL-pdf

[36]: New Cadence Tensilica Vision P5 DSP Enables 4K Mobile Imaging with 13X Performance Boost and 5X Lower Energy, Cadence Design Systems, Inc., Oct 06, 2015, https://www.prnewswire.com/news-releases/new-cadence-tensilica-vision-p5-dsp-enables-4k-mobile-imaging-with-13x-performance-boost-and-5x-lower-energy-300154540.html

[37]: Tensilica Vision P6 Processor Core Adopts Deep Learning-Focused Enhancements, BDTi, May 25, 2016, https://www.bdti.com/InsideDSP/2016/05/26/Cadence

[38]: Efland, G. et al., High Performance DSP for Vision, Imaging and Neural Networks https://www.hotchips.org/wp-content/uploads/hc_archives/hc28/HC28.22-Monday-Epub/HC28.22.40-Vision-Image-Epub/HC28.22.430-Vision-Neural-Net-GregEfland-Cadence-v02-57.pdf

[39]: Cadence Boosts Vision and AI Performance with New Tensilica Vision Q6 DSP iP, Cadence Newsroom, April 11, 2018, https://www.businesswire.com/news/home/20180411005039/en/Cadence-Boosts-Vision-AI-Performance-New-Tensilica

5. References (6)

[40]: McLellen P., A New Era Needs a New Architecture: The Tensilica Vision Q6 DSP, Cadence, April 11, 2018, https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/q6-announcement

[41]: Frumusanu A., MediaTek Announces New Premium Helio P90 SoC, AnandTech, Dec. 13, 2018, https://www.anandtech.com/show/13718/mediatek-announces-new-premium-helio-p90-soc

[42]: Padla R., MediaTek Helio P90 chipset benchmarked on AnTuTu, Android Community, Dec. 28, 2018, https://androidcommunity.com/mediatek-helio-p90-chipset-benchmarked-on-antutu-20181228/

[43]: Meizu Note 9 will adopt waterdrop type notch, Snapdragon 6150, 48 million pixel camera, ReaMEIZU, Note 9, Jan. 7, 2019, https://reameizu.com/ceo-said-meizu-developing-note9-has-snapdragon6150-and-4800mp-camera/

[44]: Wong W., 10-core SoC Targets Premium Mobile Media Devices, Electronic Design, March 02, 2017, https://www.electronicdesign.com/microcontrollers/10-core-soc-targets-premium-mobile-media-devices

[45]: MediaTek Seemingly Backing Down on the Flagship SoC Market, XDA Developers, Nov. 10, 2017, https://www.xda-developers.com/mediatek-backing-out-flagship-soc-market/

5. References (7)

[46]: MLC e·MMC™ and Mobile LPDDR3 221-Ball MCP Datasheet, ZettaDevice Electronics Technology Co. Ltd., 12/2015, https://www.google.com/search?q=MLC+e·MMC™+and+Mobile+LPDDR3+221-Ball+MCP&oq=MLC+e·MMC™+and+Mobile+LPDDR3+221-Ball+MCP&aqs=chrome.

[47: Frumusanu A., Cadence Announces Tensilica Vision Q6 DSP, AnandTech, April 11, 2018, https://www.anandtech.com/show/12633/cadence-announces-tensilica-vision-q6-dsp